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Effect of Annealing on the Electrical Characteristics of CdO-Si Heterostructure Produced by Plasma-Induced Bonding Technique

In this work, the effect of annealing on the electrical characteristics of the CdO-Si heterojunction produced by plasma-induced bonding technique was studied. The heterojunction was consisting of n-type CdO on a p-type silicon substrate. Results showed reasonable improvement in the electrical characteristics of this heterojunction within a range of annealing temperatures, above which the heterojunction showed degradation in its characteristics. This work produces CdO-Si of much better characteristics than same heterojunctions produced by thermal evaporation technique.

Keywords: CdO-Si structure, Bulk bonding, Heterojunctions, Heat treatment

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1. Introduction

Although the main driving force for development of bonding has been production of silicon-on-insulator (SOI), several other high potential applications of bonding have emerged in microelectromechanical systems (MEMS) and as a way of integrating dissimilar crystalline materials. To reach a sufficient level of maturity, bonding procedures need to be optimized and standardized according to the application. Also, bonding requires a high-temperature annealing step after the room temperature joining, to ensure the formation of a strong and uniform bonding. This high temperature annealing is sometimes incompatible with many applications and it may cause material degradation, especially when bonding thermally mismatched materials. Back to the pioneering days, low temperature bonding procedures have been highly desirable [1].

There are many factors governing the bonding behaviour of two surfaces. First, the surfaces must be flat and smooth. Usually it is argued that surfaces can make contact only at some asperities. However, the success of bonding technique has followed the development of modern semiconductor chemical-mechanical polishing (CMP) technology [2]. The semiconductor polishing technology has reached such a level of maturity that, nowadays, commercial silicon wafers have surface roughness in the order of $10^{-6}$ m. The second parameter governing the ability for bonding is the surface chemical state and surface termination. For most semiconductors, surface preparation and cleaning techniques are well-developed and characterized. However, in silicon technology the surface chemical treatments are more standardized and established processes, as compared to, for example, compound semiconductors [3].

The basic procedure in semiconductor bonding technique starts with mirror-polished surfaces that are cleaned, plasma-activated and given their final surface termination using a combination of chemical treatments [4]. The wafers are then brought together at room temperature and if proper surface conditions apply, the solids will bond spontaneous. After room temperature bonding, a heat treatment at elevated temperature is performed to strengthen the interface bonding [5]. Typical bonding technique procedures are fully compatible with microelectronic process technologies, offering several advantages both in available processing equipment and possible applications [6].

One of the great potentials of the bonding approach is the integration of dissimilar materials. Integration of dissimilar semiconductor by heteroepitaxial growth is hampered by the difference in lattice constants. Particularly, combining III-V compounds semiconductors with highly developed silicon circuits has been pursued in recent years with the goal to incorporate photonic and high-speed devices with advanced silicon technology [7].

When the solids have been bonded together at room temperature usually the interaction, or bonding energy, is relatively weak. Therefore, a heat treatment is performed to increase the bond-strength. The annealing enhances out-diffusion
of interface trapped molecules and desorption of chemisorbed surface atoms, such as hydrogen [8]. At the same time the annealing activates formation of covalent bonds between the bonded surfaces, like solid-to-solid bonding in the case of hydrophobic bonding. The thermal treatment used to increase the bond-strength can, unfortunately, also cause severe problems in bonding technique. For instance, when bonding dissimilar materials, the thermal mismatch induced high stresses in the material. High temperature annealing also restricts the use of metal patterns and can cause diffusion of dopants [9].

Generally, the bonding requires a high-temperature annealing step to ensure the formation of strong bonding between solids, i.e. to form covalent bonds. In silicon-to-silicon bonding usually an annealing above 1000°C is required, and in bonding involving compound semiconductors, the annealing is usually performed above 600°C. Such a high-temperature annealing is incompatible with many applications. Particularly, pre-structured wafers that already contain temperature-sensitive structures cannot be exposed to the high-temperature annealing. The high-temperature annealing also induces material degradation. It can cause broadening of diffusion layers. When bonding dissimilar materials, annealing at high temperatures would induce large thermal stress due to the difference in thermal expansion coefficients [10].

In this work, the annealing of CdO-Si structure produced by low-temperature plasma-induced bonding was performed and its effect on the electrical characteristics of this structure was studied.

2. Experimental Work

The experimental details of preparing samples were presented in Ref. [11]. High purity (99.999) (100)-oriented p-type silicon wafers of 500µm thickness and 3Ω.cm resistivity were used in this work. Also, high purity (99.999) cadmium oxide (CdO) was used to form 350µm-thick samples. Both samples, Si and CdO, were washed with distilled water then rinsed in ethanol and subjected to ultrasonic waves for 10 minutes, then dried by hot air. The silicon samples were then cleaned with HF for 5 minutes to remove any residual oxides which have existed on their surfaces. Both samples were softly grinded and polished to obtain flat surfaces. Then, these samples were rinsed in ethanol to remove acids then dried to be ready for processing.

However, the bonding is very weak at room temperature and after low-temperature annealing because of the hydrogen-terminated surface. A high-temperature annealing above 520°C is necessary to desorb hydrogen from surface and enable a covalent bonding. The difference in thermal expansion between CdO and Si will induce high mechanical stress in the material when annealing the bonded samples at high-temperatures. The thermal stress degrades the material by generating defects. It can also cause cracks and completely debond. The main degradation occurs in CdO since Si is a mechanically stronger material. The samples were subjected to heating up to 800°C. The sample was heated for 5 minutes then left to return to its initial temperature within the same period of time.

3. Results and Discussion

The effect of annealing temperature on the ideality factor and spectral responsivity of the prepared CdO-Si heterojunctions was first introduced within the range (400-800)°C in order to determine the optimum value of annealing temperature, as shown in Fig. (1) and (2). Temperature of 600°C is shown to be the optimum value and this is in good agreement with the published works.

![Idenity factor vs. annealing temperature](image)

**Fig. (1)** The ideality factor of the CdO-Si heterojunction at different annealing temperatures

Wafer bonded p-n heterojunction characteristics are heavily affected by the non-ideal interface. However, a substantial improvement of wafer bonded p-n heterojunctions characteristics is usually obtained by shifting the p-n transition away from the bonded interface, either by high temperature annealing [12] or by implantation [13-14]. Alternatively, the p-n heterojunction, formed under UHV conditions and low temperatures results in an ideality factor no more than 1.18, indicates low recombination at the interface. Bonding p-n heterojunction in ambient air and subsequent high temperature annealing was seen to yield high recombination near the bonded
interface. An ideality factor of 2 was obtained and low minority carrier lifetime [15].

Fig. (2) The spectral responsivity of the CdO-Si heterojunction at different annealing temperatures

Fig. (3) shows the I-V characteristics of bonded p-n Si-CdO heterojunction. As shown, the dark current is about 50μA and the forward current is uniformly linear. The illumination current in the reverse biasing reaches a maximum of about 180μA. The bonded interface is often avoided in the electrically active region of the electronic device. However, the recombination centers of the defective bonded interface are used to control the minority carrier lifetime in power devices. These characteristics are typically enhanced compared to results obtained by other techniques [16].

In order to introduce the nature of the anisotype CdO-Si heterojunction, the C-V measurements were performed in the reverse biasing and results are presented in Fig. (4). The built-in potential was determined for the CdO-Si heterojunction to be about 0.9eV.

The spectral responsivity of the CdO-Si heterojunction was determined as a function of wavelength as shown in Fig. (5). This heterojunction responds in the 550-900nm range much more than in the range below 550nm. This cheap technique presents an advantage to produce good photodetectors for the wavelengths more than 550nm.

Integration of CdO and Si has attracted much interest since the unique properties in each material can be combined in devices or systems, such as CdO-based piezoelectric devices and optoelectronics components. The epitaxial growth of CdO on Si substrate is hampered by the difference between the lattice constants of the materials. However, using bonding for the integration, the lattice-mismatch becomes no obstacle. Unfortunately, there is a large difference in thermal expansion between CdO and Si. When bonding solids of dissimilar materials and annealing at elevated temperatures, the thermal mismatch will induce high thermal stress in the material [17].
In each material system, nature has imposed a set of physical properties, such as mobility, optical absorption, resistivity, thermal and mechanical properties. For a given application, the optimal properties may not reside in a single material but in a variety of dissimilar materials. A specific case is to combine compound semiconductor that have direct band gap and high mobility with Si that is extensively used in microelectronic applications.

The applications for integrating CdO with Si can be divided into three categories, were each category has its own constraint on interface and material properties [18].

1. The unique properties of each material are combined in devices to reach optimal performance. An avalanche photodetector, for instance, has two functions absorption of light and conversion of light into an electrical signal. Therefore, the CdO was bonded to Si substrate since the CdO has high light absorption at NIR wavelengths while Si has a much higher electron/hole ionization rate leading to higher avalanche multiplication efficiency [19].

2. Integration of CdO piezoelectric and high-speed devices with Si microelectronic circuits. Optical interconnections are very desirable since they can overcome the electrical interconnect bandwidth bottleneck. Optical communication links finds application in both rack-to-rack, board-to-board and intra and interchip connections [20]. The integration of CdO devices with Si VLSI circuits may be especially advantageous since Si is transparent at NIR wavelengths. Therefore, optical communications can take place within Si bulk, which facilitates back-surface integration of micro-optics such as beam reflectors. The most straightforward approach, flip-chip bonding, which is currently used to form hybrid optoelectronic IC’s, suffers from an inherent throughput limit when multiple optical nodes exist in each die. Furthermore, thermal stress and non-planar surface profiles present additional difficulties for vertical integrated optoelectronics [21-22].

3. Si as substrate for CdO relieves the strain from CdO substrate industry. Compound semiconductor industry has implied the need for wafers with large diameters. This is much more evident in present electronic applications than in optoelectronics. However, the increment in wafer-size has not followed the same progress and there are major concerns about the up-scaling of CdO wafer dimensions [23]. CdO has several disadvantages since it is fairly immature and the crystal quality is less than the more mature Si and GaAs technologies. Also, CdO wafers are more brittle and available only in small sizes. By implementing bonding techniques, Si could be introduced as a substrate for CdO-based materials. Si wafers offers several advantages such as its low-cost, large area, mechanical strength and high thermal conductivity.

4. Conclusions

A CdO-Si heterojunction was produced by plasma-induced bonding techniques. Electrical measurements showed reasonable enhancement in the heterojunction characteristics compared to that produced by another techniques. Annealing of the prepared samples improve the electrical characteristics much more. Despite the complexity imposed by the plasma processing system, production of heterojunctions with such enhanced characteristics has advantages of low cost and large size devices.

References