Eng. &Tech.Journal, Vol. 32,Part (B), No.3, 2014

The 4th International scientific Conference on Nanotechnology& Advanced Materials &Their Applications (ICNAMA 2013)3-4 Nov, 2013

Characteristics and Evaluation of Nano Electronic Devices

Dr .Hanan A. R. Akkar
Electrical Engineering Department, University of Technology/Bagdad
Email:dr_hananuot@yahoo.com
Sarmad Khalooq
Electrical Engineering Department, University of Technology/Bagdad

ABSTRACT

Recent developments in nanotechnology have demonstrated that it is feasible to manufacture Nano electronics devices using Carbon Nano Tubes (CNTs) because the mobility between the channels is increased while the switching delay is decreased. The devices based on Nano scale objects with well-defined structure and original electronic properties are great interest for the development of innovative electronic circuits. In this paper, a proposed design of carbon Nano tube transistors, Nano RAMS, Nano wires, Nano Flip Flops and Nano Diodes are presented. The Carbon Nano Tube Field Effect Transistor (CNT FET) leads to an area reduction, density of carbon Nano tube as well as the power consumption is decreased when it is compared with MOSFET. The comparison between Nano CMOS and CNTFET shows that CNTFET is very promising and superior technology for circuit design access time reduction with temperature increasing which is opposite to the Nano CMOS behavior delay. The results obtained are useful in characterizing and evaluating performance of Nano devices and related circuits. The results proved that CNTFET appears to be the best device in future for VLSI. The modeling and simulation has been implemented using MATLAB program.

Keywords: Nanotechnology, Nano Electronics, CMOS Technology, Carbon Nano Tubes.

تحليل خصائص العناصر النانو الكترونية

الخلاصة

يعتبر أستخدام أنابيب الكاربون النانوية من الأستخدامات الواعدة في مجال الالكترونيات في المستقبل القريب نظراً لخصائصها الإلكترونية الممتازة مثل تحملها لدرجات حرارة عالية، قوة وصلادة كبيرة ، حركية عالية، توصيلية كهربائية جيدة والتوافق مع المواد ذات العازلية العالية وبأقطار صغيرة. تم درا سة أنابيب الكاربون وأنواعها المختلفة. حيث تم تصنيف أنابيب الكاربون الى نوعين أساسين وهي الأنابيب الكاربونية النانوية ذات الجدار الواحد(SWCNT) وأنابيب الكاربون متعددة الجدار(MWCNT) ومقارنتها, حيث تم اختبار تطبيقات أنابيب الكاربون لتصميم ترانزستور نوع (CNTFET) بانواعه المختلفة، الصمام الثنائي النانوي، المفتاح النانوي، بوابة النانو، نانو RAM، نطاطات النانو حيث تم تصميم هذه الانواع بالاعتماد على CNTFET. تم تحليل خصائص الترانزستور باستخدام برنامج المحاكاة الحاسوبية للمقارنة مع الانواع التقليدية، حيث تبين إمكانية عملها بتيارات قليلة تصل إلى النانو أمبير 1nA مقارنة مع ألانواع التقليدية التي تستهلك طاقة أقل.

أجريت مقارنات بين CNTFET، MOSFET، نانو CMOS، بمساعدةالمختبر الرياضي MATLAB حيث بينت النتائج تفوق CNTFET من حيث السرعة والحد من وقت وصول أكثر من غير ما هوعليه حيث يمكن أعتبارCNTFET أفضل عنصر للعمل بالمستقبل في VLSI.

INTRODUCTION

Nanotechnology is the first major worldwide research initiative of the 21st century that acts as both the basis for technology solutions across a range of industrial problems or as a related for the convergence of other enabling technologies like biotechnologies, computational sciences, physical sciences, communication technologies, cognitive sciences, social psychology and other social sciences. Semiconductor industry is ready to downscale Complementary Metal Oxide Semiconductor (CMOS) transistors which has formed denser, cheaper, faster, smaller, and functionality richer electronic devices. However, further scaling becomes more challenging with any new technological node as CMOS physical gate length which has reached the nanometer geometry scale (1–100 nm). Nano scale CMOS devices start to be influenced by quantum mechanical properties effects. Furthermore, manufacturing problems in patterning small size transistor, increasing cost in creating the chip and increasing in power density dissipation are some other problems faced by semiconductor industry. These are the causes that CMOS devices are predicted to end their services at the end of next decade. This technology base was first discussed in the last half of the 20th century technically by Fynman in 1960 and commercially by Drexler in 1986 and took decades to generate significant public investment with huge public investments to support scientific researches [1]. Therefore, literature survey for many previously published researches is presented as follows:-

S. D. Pable, et al, investigates the performance analysis of sub-threshold circuits, improves in speed of logic gates using CNFETs, investigated the characteristics of CNFETs in Sub-threshold region [2]. S. Salahud Din, et al, characterize the main CNTFET performances on-current (Ion), Ion/Ioff ratio and inverse sub threshold slope S according to the dispersion on the nanotube diameter [3]. K. Hess, et al, proposed a semi-classical model for the performance investigation and optimization of the double gate carbon nanotube field-effect transistor (DG-CNTFET) [4]. Finally C. Chen, et al, compare a multi channel of CNTFET with the single-channel CNTFET in terms of ON current, trans conductance, switch performance and also the reliability and yield of the device [5]. CMOS transistor scaling and performance will continue at least until the middle of the next decade. Recently, a lot of interest generated has been generated and good progress has been made in the study of novel silicon and non-silicon Nano electronic devices, including Nano wire, Field Effect Transistors FET, carbon Nano tube FET [6].

Nano devices can be classified, based on the phenomena driving their operation into three classes namely electrical-dependent, magnetic-dependent, and mechanical-dependent. The electrical-dependent Nano devices are based either on ballistic transport, tunneling or, on electrostatic phenomenon. In the case of ballistic transport the electrons travel without resistivity in a material. In the case of tunneling, the electrons can pass through a potential energy barrier at some level of energy as results of a quantum-mechanical process. In the case of electrostatic, the interaction of electrons happens with the presence of electric field. Integrated circuit doubles every 24 months, and it has been the guiding principle for the semiconductor industry for

over 30 years the sustaining of Moore's Law, however, requires continued transistor scaling and performance improvements [7].

In this paper a proposed design of carbon Nano tube transistors, Nano RAMS, Nano wires, Nano Flip Flops, and Nano Diodes are presented. The Nano electronic device which is formed from CNT proved that it is better than ordinary devices. Generally, these Nano devices have some advantages compared to CMOS transistors, for instance, higher mobility electrons, smaller size, and lower power consumption. On the other hand, there are some disadvantages, for example, low temperature requirement, immature fabrication techniques, and vulnerable to noise due to low power operation. In the following subsections, we explain the basic concept of operation, advantages, disadvantages, and present the current analysis for each Nano device considered in this paper.

DESCRIPTION MODELS OF CNT

Interconnect for integrated circuits have traditionally been fabricated out of metals like copper and aluminum. However, with the continued downscaling of the cross section, alternative possibilities are being considered. Perhaps the most well-known are metallic carbon nano tubes for which a novel transmission-line model has been proposed which were applied by Burke to evaluate potential applications. Recently, a performance comparison between metallic CNTs and Cu wires was done regarding their interconnect applications based on Burkes study [8].

One way to increase the speed of the nano wires is to increase the number of modes or the number of sub bands. Geometrically, the number of sub bands is limited by the diameter and band structure of the specific nano wire. For a given dimension for the nano wire, it may be worthwhile to examine how a parallel combination of many nano wires, occupying the same amount of space as conventional interconnects, compare with them in performance. For a specific example, let us choose the metallic carbon nano tube. For simplicity, we shall assume that when we put the metallic CNTs in parallel, they are no interacting in nature. For low field transport we shall assume a mean-free path ƛ=1.6μm estimated from experimental data. For high field transport electrons require a finite length, Lt travel before they acquire the energy (0.16 eV) to emit an optical phonon [9]. Then the total length that the electron travels is $(Lt + Lhp)\ where\ Lhp = \ \mathbf{30}\,nm$. The resistance of a metallic CNT can be modeled as:

$$\mathcal{R} = \left(\frac{\hbar}{4e^2}\right)\left[1 + \frac{L}{\lambda acc}\right] \qquad \text{Low field} \qquad \ldots (1)$$

$$\mathcal{R} = \frac{h}{4e^2\left[1+L\left(\frac{1}{\lambda acc}+\frac{1}{\frac{0.16L}{v}+Lhp}\right)\right]} \qquad \text{High field} \qquad \ldots (2)$$

Where L is the length of the wire, v is the applied voltage and L = 0.16L/V. We have assumed that V=0.5v for the high field transport, the effect of ballisticity of CNTs is evident. The nanotube resistivity is only affected by the contact resistance up to a significant length.

CNTFET which is closely similar to MOSFETs in terms of construction and operation the only difference is that the channel is formed using CNT wire instead of

the bulk substrate as shown in Figure (1) [10]. The type of electrodes that used CNTFET is classified into three categories the Schottky-barrier (SB) CNTFET, Partially gated (PG) CNTFET and doped-S/D CNTFET as illustrated in Figure (2).

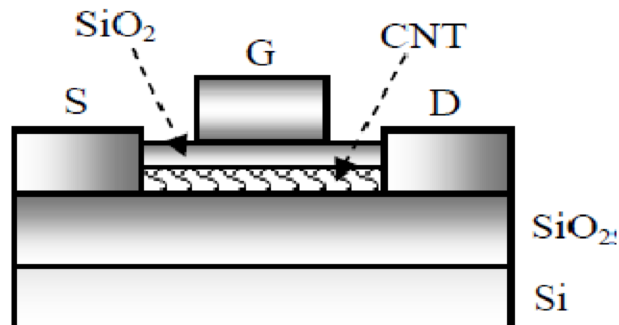


Figure (1) Schematic structures a CNTFET [10].

The Schottky-barrier (SB) CNTFET is shown in Figure (2a), where, in this type of CNTFET an intrinsic CNT is used in the channel region. This is connected to metal Source/Drain and forms Schottky barrier sat the junctions. Carbon nano tube transistors operate as unconventional Schottky barrier transistors in which transistor action occurs primarily by varying the contact resistance rather than the channel conductance. These types of FET require careful alignment of the Schottky barrier and gate electrode which leads to manufacturing challenge. Also the presence of Schottky barrier lowers the on-current [11].

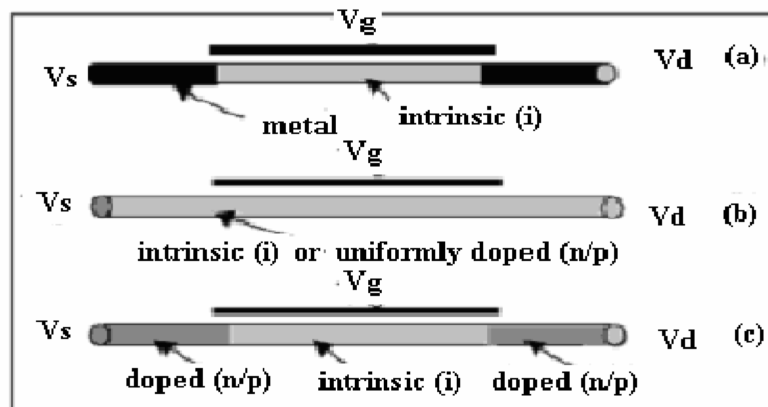


Figure (2) Different types of CNTFET: (a) Schottky-barrier (SB) CNTFET, (b) Partially gated (PG) CNTFET (c) doped-S/D CNTFET [11].

The Partially Gated (PG) CNTFETPG-CNTFET, shown in Figure (2b), is a depletion mode CNTFET in which the nano tube is uniformly doped or uniformly

intrinsic with ohmic contacts at their ends. PG-CNTFETs can be of n-type or p-type when respectively n-doped or p-doped. In these devices the gate locally depletes the carriers in the nano tube and turns off the p type (n-type) device with an efficiently positive (negative) threshold voltage that approaches the theoretical limit for room-temperature operation. The on-current of such devices is given as ID (on) = q ρ vt where ρ is the carrier density per unit length and vt is the unidirectional thermal velocity [11]. The Doped- Source or Drain (S/D) CNTFET presented in Figure (2c) are composed of three regions. The region below the gate is intrinsic in nature and the two unrated regions are doped with either P-type or n-type. The ON-current is limited by the amount of charges that can be induced in the channel by the gate and not by the doping in the source. They operate in a pure p- or n-type enhancement-mode or in a depletion-mode, based on the principle of barrier height modulation when applying a gate potential. The current voltage curve can be divided into two regions: linear and saturation. Drain current in the linear region of CNTFET can be described as follows:-

$$\mathbf{Id} = \frac{\mathbf{W}}{\mathbf{L}} \mu \, \mathbf{Cox} \left[(\mathbf{Vgs} - \mathbf{VT})\mathbf{Vds} - \frac{\mathbf{Vds}^2}{2} \right]$$

Or

$$Id = Kn\,[2(Vgs-VT)\,Vds-Vds^2/2] \quad \ldots(3)$$

Where Kn is conductance of CNTFET, W is the width of CNTFET, L is the length of CNTFET, μ is mobility of carriers, Cox is gate capacitance. We can also obtain saturation current of CNTFET by replacing Vds (sat) = Vgs – VT. Then the expression of saturation current of CNTFET can be written:

$$\mathbf{Id(sat)} = \mathbf{K}n(Vgs - VT)^2 \quad \ldots(4)$$

The Applications of CNTFET in order to demonstrate the veracity of CNTFET; we employed it to design various digital circuits such as Nano logic gates, Nano flip flops, NanoRam, Nanocounter circuit etc. Figure (3) shows an exemplary logic gate (inverter) comprising of P-type and N-type CNTFETs. They are coupled together in series between a high supply voltage (VDD) and a low supply reference VSS, as shown. The first CNTFET which is biased to conduct holes, functions as a driver transistor with its gate providing an inverter input VIN. The second transistor which is biased to conduct electrons, functions to facilitate an active load with its gate coupled to a supply VGG for appropriately biasing it, so that the output provides suitable low and high values when VIN is high and low respectively.

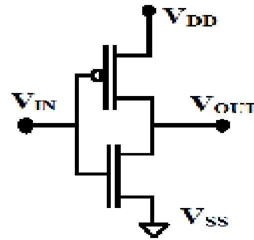


Figure (3) Structure of Nano NOT gate [12].

Figure (4) shows an exemplary Nano NAND gate comprising of CNTFETs. It comprises of driver CNTFETs coupled together in parallel between a high supply reference (VDD) and a series active load transistors, which is coupled to a low supply reference VSS, as shown the gates of the driver transistors provide first and second NAND gate inputs respectively and a gate output is provided at the drain of third transistor as shown. Either input or any one of the inputs LOW (e.g., 0V) then the output is HIGH (approaching VDD); if both inputs are HIGH, then the output will be LOW.

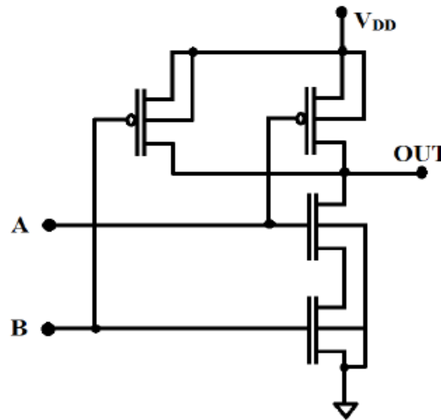


Figure (4) Structure of 2 inputs CNTFET NAND gate.

Nano RAM (NRAM) is a nonvolatile NEMS memory device formed by suspending a metallic CNT over a trench which contains a base electrode. The off state is characterized by the CNT lying flat across the trench where elastic energy keeps the tubes in place. The on state occurs when the CNT is bent into the trench and makes contact with the base electrode. In the on state, the van derails force between the CNT and the trench floor creates a strong molecular attraction, overpowering the elastic energy. Since these interactions are purely molecular, no power is consumed when the memory is at rest. Programming is accomplished by applying either attractive or repulsive voltages at the CNT and base electrode. This creates an electro-mechanically switchable [11]. The benefits of Nano RAM are permanently nonvolatile, high speed similar to DRAM/SRAM, High density similar to DRAM and UN limited life time.

SIMULATION RESULTS AND DISCUSSION

MATLAB program was written to implement equations (1) and (2) where, Figure (5) shows the algorithm for Metallic CNT wire which is depend on two equations (1 and 2) for low field and high field. As a result in Figure (6), the upward turn of the resistivity curve occurs much later for a CNT compared to the Cu wire. This is why CNT shows a smaller resistance compared to Cu wires for larger lengths. For very short lengths the resistivity for CNT is higher due to higher contact resistance resulting from smaller number of modes compared to the Cu wire. The bottom line is, if enough CNTs can be put in parallel, the performance may be comparable or better than the Cu wire.

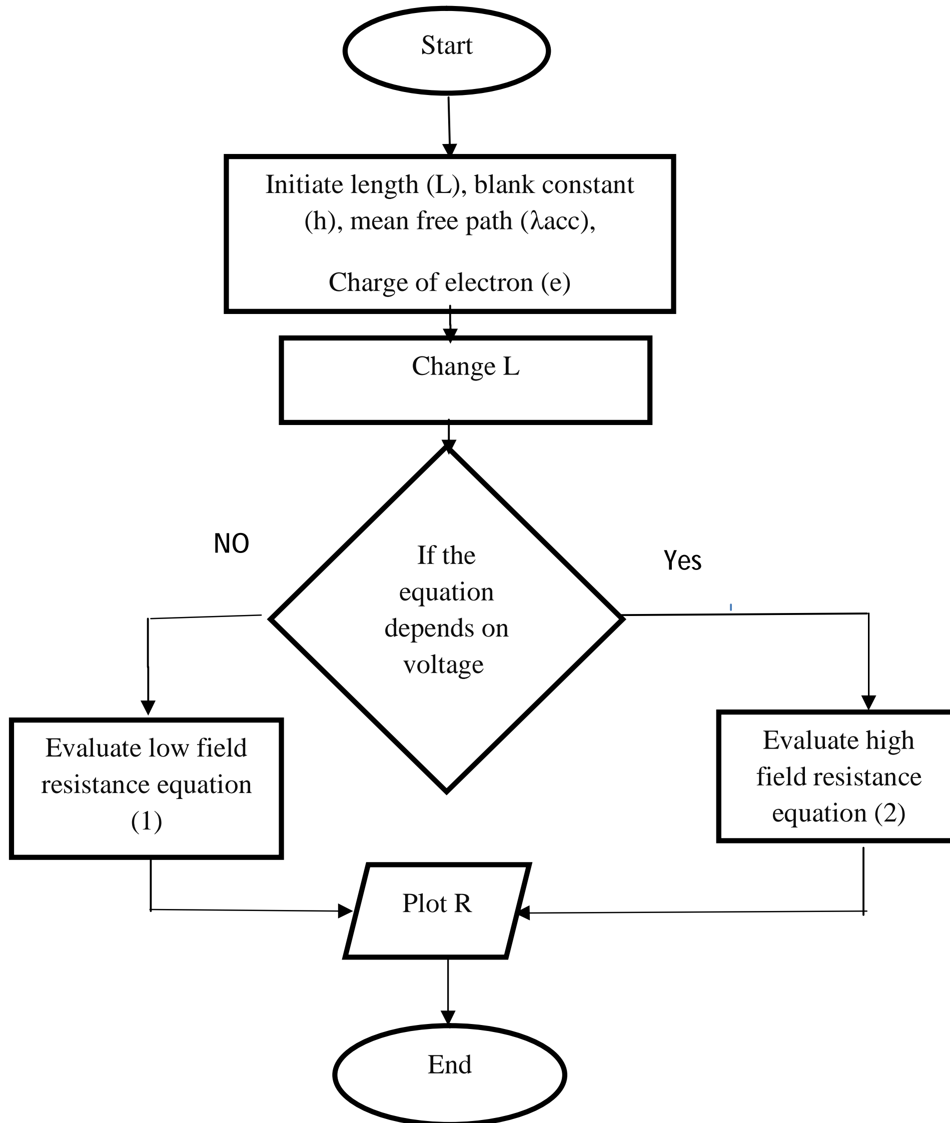
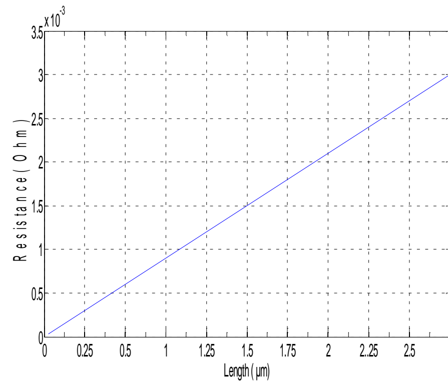
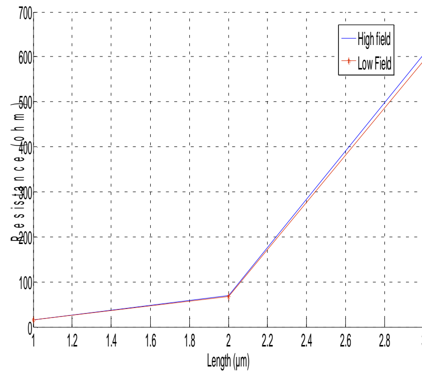


Figure (5) Flowchart of Metallic CNT Wire to simulate equation1 and equation (2).



(a)



(b)

Figure (6) MATLAB results of resistance (a) length of metallic CNTs (b) Cu interconnect.

MATLAB program was written to implement equations (3 and 4) where, Figure (7) shows the algorithm for CNTFET characteristic which is depend on two equations first represent the operation of CNTFET in linear region and second represent the operation of CNTFET in saturation region.

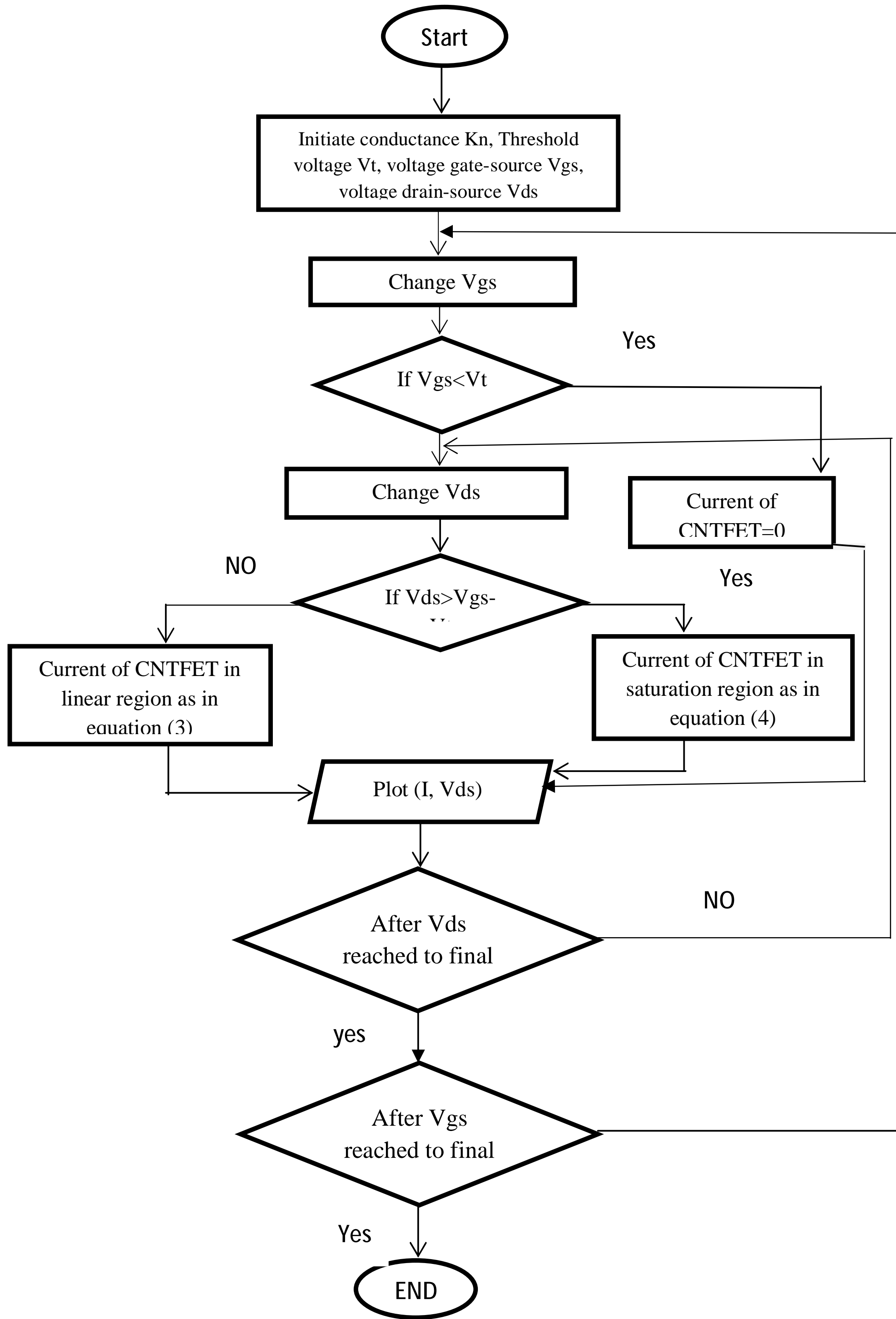


Figure (7) Flowchart of CNTFET Characteristics.

Used MATLAB to simulate the characteristics of the transistor implemented using three different technology models as shown in Figures (8, 9 and 10). In case of Si-MOSFET switching occurs by altering the channel resistivity but for CNTFET switching occurs by the modulation of contact resistance. CNTFET is capable of delivering three to four times higher drive currents than the Si MOSFETs at an overdrive of 1 V. CNTFET has about four times higher trans conductance in comparison to MOSFET. The average carrier velocity in CNTFET is almost double that in MOSFET. The on-current performance advantage of the CNTFET is either due to the high gate capacitance or due to the improved channel transport. The improved channel velocity for the CNTFET is due to the increased mobility and band structure of CNTFET.

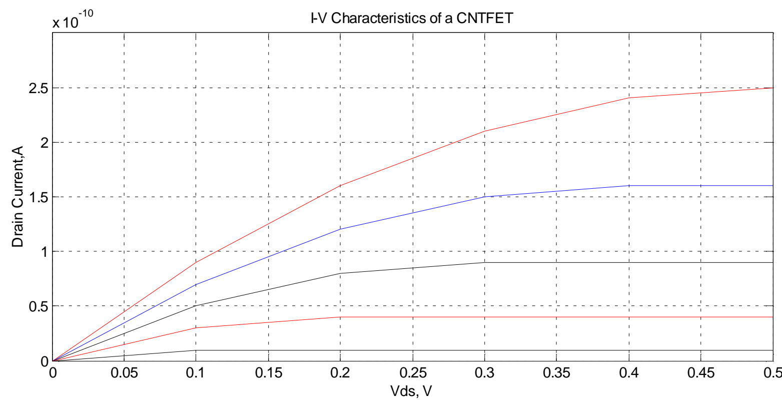


Figure (8) Current voltage characteristics for different value of Vgs in CNTFET.

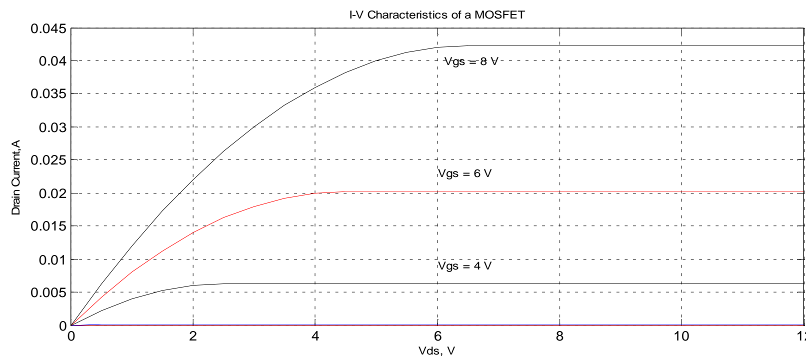


Figure (9) Current voltage characteristics for different value of Vgs in (MOSFET).

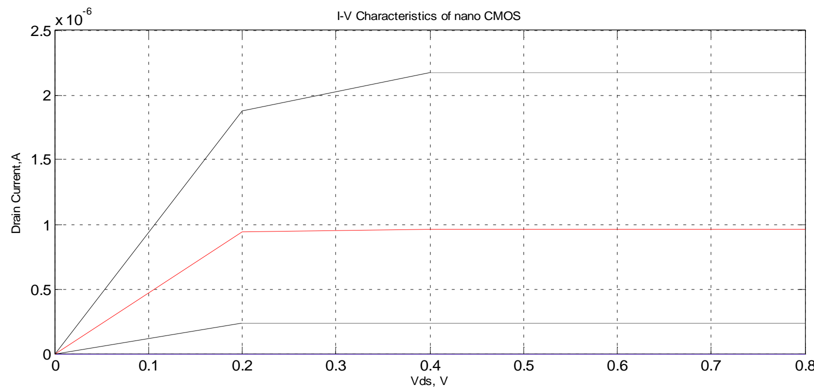


Figure (10) Current voltage characteristics for different value. of Vgs in Nano (CMOS).

CONCLUSIONS

In this paper, different Nano devices were discussed, The Nano devices are classified into three distinct classes based on the physical phenomena behind their operation. A detail overview of the operation, the advantages, the disadvantages, and the applications of each device has been discussed. Also Nano electronic devices including Nano wire & (CNTFETs) were discussed. (CNT) was used as a channel in between the source and drain to use the benefit of high mobility. A better I-V characteristic was obtained with higher mobility in between the channel and used dielectric layer. (CNTFETs) first compared with MOSFET& produced denser, cheaper, faster, smaller, and functionality the performance advantages richer electronic devices. Second the (CNTFETs) was compared with Nano CMOS show a clear superiority of the CNTFET and access time reduction than in Nano CMOS, then CNTFET is the best device for future in the VLSI.

REFERENCES

[1]. Nor Zaidi Haron, Said Hamdioui, and Sorin Cotofana, "Emerging Non-CMOS Nano-electronic Devices- What are they?" 7th IEEE International, 2009.

[2]. S. D. Pable, et al, "Nanoelectronics and Nanosystems: From Transistor to Molecular and Quantum Devices", Springer-Verlag, 2009.

[3]. Salahud din, S. et al, "Transport Effects on Signal Propagation in Quantum transactions on electron devices, Vol. 52, No. 8, August, 2010.

[4]. Hess, K. et al, "Theory and applications of near ballistic transport in semiconductors", Proceedings of the IEEE, Vol. 76, No. 5, pp. 519–532, May, 2008.

[5]. Chen, C. et al, "Carbon Nanotube Field-Effect Transistors for High-Performance Digital Circuits— Transient Analysis, Parasitic, and Scalability", IEEE Transactions on electron devices, Vol. 53, No.11, November, 2011.

[6]. Anuj Pushkama, et al, "Comparison of Performance Parameters of Scram Designs in 160m CMOS and CNTFET Technologies", IEEE, 2010.

[7]. Park, J. Y. S. Rosenblatt, Y. Yaish, H. UstUnel, S. Braig, T. A. Arias, P. W. Brouwer, and P. L. McEuen, "Electron-phonon scattering in metallic single-walled carbon nana tubes," Nano Let., Vol. 4, No. 3, pp. 517–520, 2009.

[8]. Naeemi, A. R. Savari, and D. Meindl, “Performance Comparison between Carbons Nanotube and Copper Interconnects For Gsi,” in IEDM Tech. Dig., pp. 699–702, 2004.

[9]. Rasmita Sahoo and R. R. Mishra, "Simulations of Carbon Nanotube Field Effect Transistors", 6450 Vol. 1 No. 2 pp. 117–125, (2009).

[10]. DinhSy Hien1, Nguyen Thi Luong1, Thi Tran Anh Tuan 1 and Dinh Viet Nga1,"Modeling of planar carbon nana tube field effect transistor and three dimensional simulation of current-voltage characteristics", Journal of Physics: Conference Series 187 (2009).

[11]. Sridevi, V. T. Jayanthy, "Carbon Nanotube Field Effect Transistor Based Mod-16 Counter” international Journal of Scientific Research, Vol.67, No.1, ISSN 1450-216 X pp119-127, (2011).

[12]. Scott Chilstedt · Chen Dong · Deming Chen, "Design and Evaluation of a Carbon Nano tube-Based Programmable Architecture", Int. Journal of Parallel Progress 37:389–416, 2009.