FPAA IMPLEMENTATION OF CHAOTIC MODULATION BASED ON NAHRAIN MAP

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***Abstract*– Due to characteristic of chaotic systems in terms of nonlinearity, sensitivity to initial values, and non-periodicity, they are used in many applications like security and multiuser transmission. Nahrain chaotic map is an example of such systems that are recently proposed with excellent features for the use in multimedia security applications. Although the implementation of chaotic systems is easy using low cost analogue ICs, this approach does not provide the flexibility that the reconfigurable analogue devices have in design possibilities such as reducing the complexity of design, real-time modification, software control and adjustment within the system. This paper presents a description of data modulation and demodulation based on Nahrain chaotic system and there hardware implementation using field programmable analogue array (FPAA) device. AN231E04 dynamical programmable Analog Signal Processor (dpASP) board is used as a target device for the implementation. The simulation results of system closely matched the programmable hardware testing results.**

Keywords: **FPAA, Social media analysis, Nonlinear, Discrete System, Nahrain Chaotic System, Modulation**

I. INTRODUCTION

Chaotic system of simple structure can demonstrate complex dynamical properties in infinite mathematical world, such as sensitivity to initial conditions, topological transitivity and mixing, expansiveness, and decaying autocorrelation function [1]. Due to its wideband nature, a modulation scheme using chaotic basis functions is potentially more resistant to multipath propagation than one based on sinusoid [2]. So, designing chaos-based transmission schemes emerged as a new research direction to reinforce information security of data sent through the Internet. In chaos-based digital communication systems, digital symbols are mapped to non-periodic chaotic basis functions with various coherent and non-coherent communication schemes. As a chaos based digital communication scheme, Chaos shift keying (CSK) has gained much interest among researchers with less complexity with better noise immunity to modulate digital symbols with chaotic basis signals [3].
The transmitter and receiver blocks of CSK communication system are presented in Fig.1. A message is transmitted by changing one or more parameters of the transmitter dynamics which results in a change of the attractor dynamics. At the receiver, the message is demodulated by estimating to which message the received chaotic attractor corresponds. The transmitter consists of M chaos generators. In the case, when we use a binary message, only two chaos generators are required. In Fig.1, the transmitter consists of two chaos generators A and B, producing signals C0(t) and C1(t), respectively [4]. If a binary symbol "0" is to be sent, C0 is transmitted by the communication channel, and if the binary symbol "1" is to be sent, C1 is transmitted [5].
CSK requires coherent receivers in order to regenerate an exact replica of the chaotic sequence. On other hand, the signal processing is implemented through digital devices such as programmable logic devices like FPGA (Field Programmable Gate Arrays), CPLDs (A complex programmable logic device), microcontrollers, etc., that kept analog signal processing out of modern trends in programmable devices. Recently, a number of researches have been done in the field of reconfigurable analog signal processing using Anadigm dpASP, and PsoCs. An FPAA is an analog equivalent of the FPGA. With this

technology the complexity and time effort of the analog circuit design is minimized. It seems that the FPAA devices can be used in a simple signal processing realizations like: filtering, control, sensor linearization [6]. Some of the manufactured devices have ability to dynamically change the configuration, what opens a feature to the robust and adaptive hardware [7]. The paper is organized as follows. Section 1 presents the current stage of hardware implementation of chaotic transmission system. Section 2 outlines the related works of implementing data transmission based on chaotic system. Section 3 presents the hardware implementation of Nahrain chaotic map. Section 4 presents the hardware implementation of chaotic modulation based on Nahrain chaotic map. Section 5 includes hardware implementation. Section 6 includes the simulation and hardware results of the system. Finally, section 7 gives the conclusions of the paper.

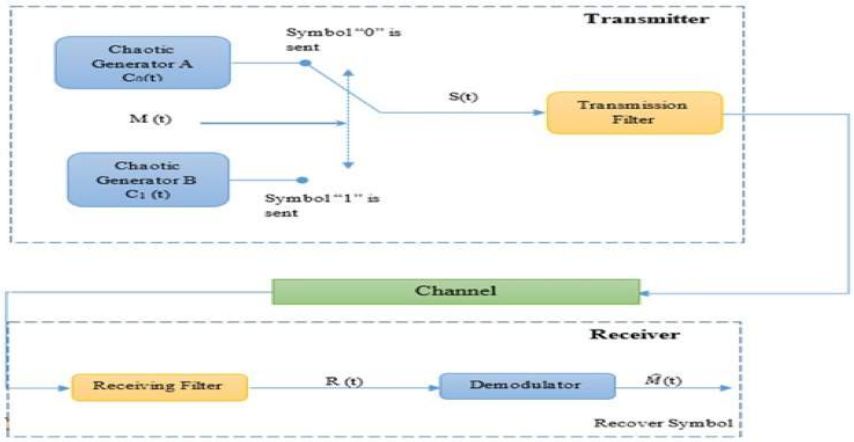


Figure 1: Binary chaos shift keying digital communication system

II. Related Works

There are many chaotic system implementation using FPAA in literature. In 2014, a new dual entropy core true random number generator (TRNG) capable of producing high levels of randomness using hardware redundancy is proposed. Comparative analysis of the statistical and randomness properties have been performed for developed traditional and proposed TRNG architectures. FPAA is used for design and hardware implementation of the proposed model [8]. Analog programmable electronic circuit-based chaotic Lorenz system is introduced in [9]. The design and hardware implementation of the system is achieved using FPAA. The experimental results demonstrated that the circuit exhibits pre-chaotic transient and chaotic Lorenz attractor. In 2016, a random number generation method based on based on a piecewise linear one dimensional (PL1D) discrete time chaotic maps for applications in cryptography and steganography is proposed. The proposed system is practically implemented by using FPAA-FPGA [10]. In 2017, linear synchronization and circuit implementation of chaotic system with complete amplitude control based on FPAA is proposed [11]. A performance comparison study of programmable platforms: FPAA and FPGA implementation of Chaos On/Off Keying (COOK) Communication System is given in [12]. In 2018, we have proposed a new dynamical system called Nahrain chaotic system [13]. We proved that it has excellent performance for multimedia encryption and secure transmission [14]. However, in [13] we have only

presented a part of the standard randomness tests to prove the system randomness behavior. In this paper, we will review Nahrain chaotic system and complete the presentation of its FIPS 140-2 randomness tests. Then we will introduce the implementation of the system using programmable hardware to allow the system dynamics, reconfigurable and achieve rapid experimental setup with low cost. For this purpose, AN231E04 FPAA device from Anadigm Inc, the latest production of Anadigm's dpASP series is used as target device.

III. N CHAOTIC MAP

The nonlinear equations that describe Nahrain chaotic system are [13] :

$$\begin{aligned} X_{n+1} &= 1 - X_n Y_n - x_n^2 \\ Y_{n+1} &= X_n \\ Z_{n+1} &= Y_n - bZ_n \end{aligned} \tag{1}$$

The system consists of state variables: X, Y and Z and two parameters: a and b. Through a series of numerical modeling and simulation associated with MATLAB, the phase portraits of chaotic behavior have been acquired by using system parameter values: a=1.52 and b=0.05. The schematic block diagram of Nahrain chaotic generator is shown in Fig.2.
Figure 3 shows the phase portraits of the system when its initial conditions are: X(0)=0.3, Y(0)=0.2 and Z(0)=0.1. It is clear from this figure that the attractors have strange shape which meets the well-known properties of chaotic behavior. The other numerical and statistical tests required to confirm this behavior will be presented and applied for Nahrain system in the next two sections respectively.

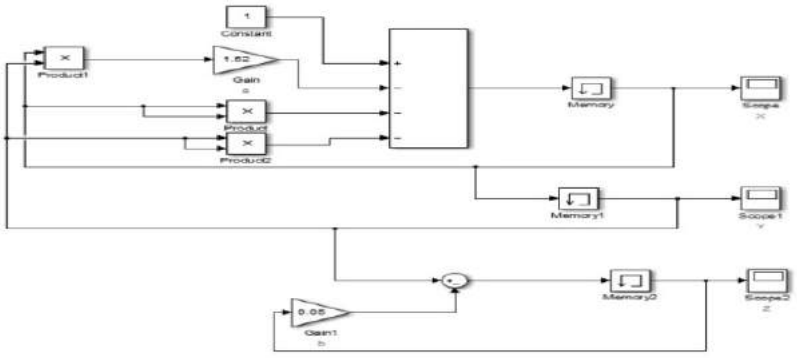


Figure 2: Matlab-simulink implementation of nahrain chaotic map

1) Performance Analysis Tools for Nahrain Chaotic System: The behavior chaotic system is very useful in security system to disorganize the communication data in order to increase security requirements. To prove the behavior of proposed system, there is a number of system's statistical analysis that presented and discussed. These analysis are categorized into

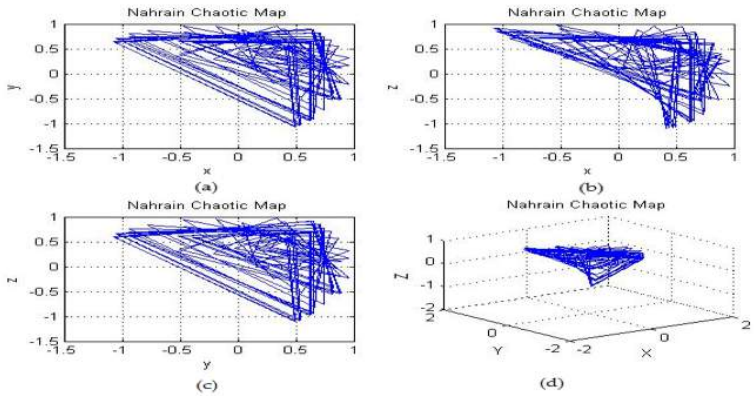


Figure 3: Phase portraits of the proposed chaotic system: (a) X-Y, (b) X-Z, (c) Y-Z, (d) X-Y-Z

two groups. The first group includes the tests that verify whether the system is chaotic or not. The second group includes the tests that are used to verify the randomness properties of the system according to the key that is created from the system.

2) Chaotic Behavior of Dynamic System Tests: Lyapunov exponent and 0-1 tests of any dynamical system are mathematical quantities used to measure the system behavior whether it is chaotic or not. 0-1 test is presented by Gottwald and Melbourne [12]. The input numbers used in the tests are the keys generated from the dynamic system in time domain and the output is a number between 0 to1. The algorithm of the 0-1 test could be explained as follows:

1. Assume a set of data f(n) sampled in time n, where n =1,2,3 N, which represent a one dimensional data.
2. Choose a positive real constant number r.
3. Compute p(n) and s(n) as using the following equations:

$$p(n) = \sum_{j=1}^{n} f(j)\cos(jr) \tag{2}$$

$$s(n) = \sum_{j=1}^{n} f(j)sin(jr) \tag{3}$$

4. Calculate the mean square displacement M(n) as follows

$$M(n) = \lim_{N\to\infty} \frac{1}{N} \sum_{j=1}^{n} [p(j+n) - p(j)]^2 + [s(j+n) - s(j)]^2 \tag{4}$$

5. The asymptotic growth rate is defined as:

$$K = \frac{logM(n)}{\log n} \tag{5}$$

The value of K for continuous system defines the system whether chaos or not, where K 0 denotes that, the system is not chaotic (ordinary), while K 1 denote that, the system is chaotic.

3) The Randomness Tests: The randomness tests are used to prove the randomness of chaotic random bits sequence CRBS. The standard randomness test FIPS 140-2 are well known test standard. If any CRBS passes the specified tests can be pretended as a good CRBS. The following tests are implemented on sequence of 15,000 bits of output from the generator [13]

1. Frequency (Monobit) Test: This test interest to the ratio of ones and zeroes for the whole sequence. The test objective is to evaluate the nearness of zeros to 1 / 2, which means that the ones and zeros in whole range is the same. All next tests rely on the crossing of this test.

2. Frequency Test Within a Block: This test interest to the ratio of ones in a block with M-bit size. The test objective is to define if the frequency of ones in an M-bit block is near M/2 or not.

3. Runs test: This test interest to the overall number of runs in the sequence (run is a continuous sequence of congruous bits).

4. Longest Run of Ones in a Block Test: This test interest to the longest run of ones within M-bit blocks.

5. Binary Matrix Rank Test: This test interest to the rank of separated sub-matrices of the complete sequence.

6. The Discrete Fourier Transform (Spectral) Test: This test interest to the peak heights in the discrete fourier transform of the sequence.

7. Maurer's (Universal Statistical) Test: This test interest to the number of bits between matching patterns.

8. Approximate Entropy Test: This test interest to the frequency of all possible overlapping m-bit patterns across the whole sequence.

9. Cumulative Sum Test: This test interest to determine whether the cumulative sum of the partial sequences is too large or too small compare to the redicted behavior of that cumulative sum for random sequences.

10. Random Excursions Test: This test interest to the number of cycles having exactly K visits in a cumulative sum random walk.

11. Random Excursions Variant Test: This test interest to the total number of times that a specific state is appeared in a cumulative sum random walk.

In all above tests, P-value is calculated to define the strength of the evidence against the null hypothesis. For these tests, each P-value is the probability that an ideal random number generator would generate a less random sequence than the sequence that has been tested, given the type of non-randomness estimated by the test. If a P-value of the test is equal to 1, this means the sequence has ideal randomness while if P-value is equal to zero this means the sequence is totally non-random. A threshold value (α) can be chosen for the tests. If P-value > α, the sequence is random. If P-value< α, the sequence is non-random. Typically, is in the range [0.001, 0.01].

IV. THE PROPOSED CHAOTIC MODULATION METHOD

In this work, the carrier signal used is Nahrain chaotic map. Each single information bit is mapped into appropriate analog chaotic patterns where each bit is represented by different outputs of the chaotic system. At the receiver end, the sample functions are correlated in the receiver and the decision is made by threshold comparison. The receiver is composed of chaotic synchronization controller, correlator, and decision device. The CSK modulated signal is expressed as:

$$s(t) = \begin{cases} X(t) \ for \ data \ 1 \\ -Z(t) \ for \ data \ 0 \end{cases} \tag{6}$$

In this type, bit 1 is represented by x(t), while bit 0 is represented by z(t). At the receiver side, the outputs of correlator1 and correlator2 are s1 and s2 respectively:

$$s1 = \sum_{t=0}^{T} r(t)X(t) \tag{7}$$

$$s2 = -\sum_{t=0}^{T} r(t)Z(t) \tag{8}$$

The original binary signal is recovered using the decision rule:

$$b(t) = \begin{cases} 1 \ if \ s1 \geq s2 \\ 0 \ if \ s1 < s2 \end{cases} \tag{9}$$

V. HARDWARE IMPLEMENTATION

AN231K04 development board is used as hardware device for implementing the chaotic modulation system based Nahrain chaotic map. The AN231K04 development board is one of the latest production of Anadigm's dpASP. The flow chart of a model FPAA implementation is shown in Fig.4. The diagram shows the system are firstly tested numerically simulation before implementing it on an FPAA. Then the mathematical system is modeled by Anadigm Designer2 software. After that, the model of the system is downloaded to FPAA board using Anadigm Designer2 software. The results obtained from programmed hardware are then compared with simulation results. If there is a difference between hardware and software results, it is discarded by modulating the system model using Anadigm Designer2 software. The implementation is completed when all the different are discarded. The implementation of the proposed system is divided in to two parts, the first part is the implementation of the Nahrain chaotic map generator and the second part is the implementation of chaotic modulation and demodulation.

1) Implementation of Nahrain Chaotic System: According to the Simulink model that presented in Fig.2, Nahrain discrete chaotic system is built using configurable analog modules (CAMs) in Anadigm Designer2 as shown in Fig.5 and downloaded to the development boards. Due to limited capacity of FPAA board, two boards are needed to realize the chaotic system. CAM values for FPAA1 and FPAA2 are given in Table I.

2) Implementation of Chaotic Modulation and Demodulation Based on Nahrain Map: The chaotic modulation system described by equations 6-9 was built using CAMs in Anadigm Designer2 as shown in Fig.6 and downloaded to the development board. CAM values for FPAA1 and FPAA2 are given in Table II.

VI. EXPERIMENTAL MEASUREMENTS RESULTS

The experimental results of Nahrain chaotic system consist of two parts: the simulation results and hardware test results. These results are presented in the next sections.

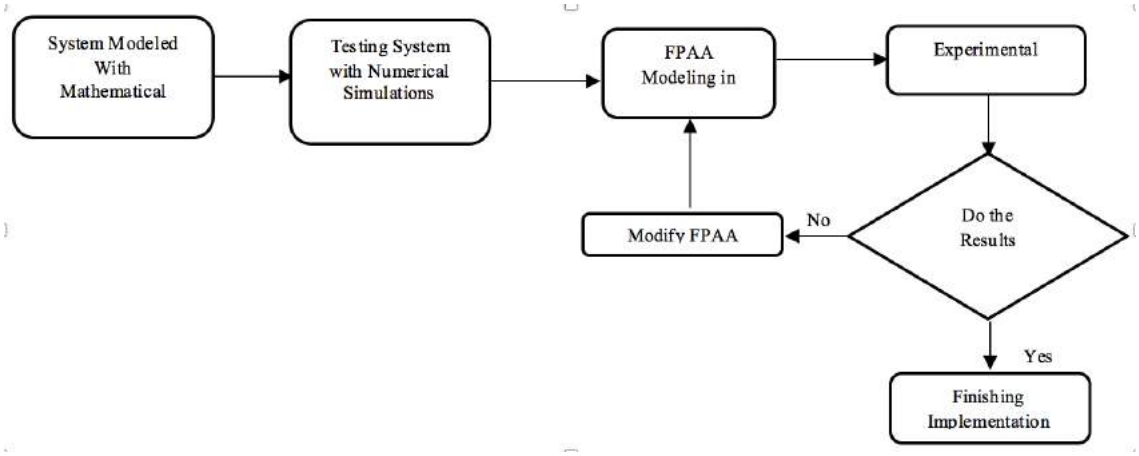


Figure 4: The flow diagram of a typical FPAA implementation

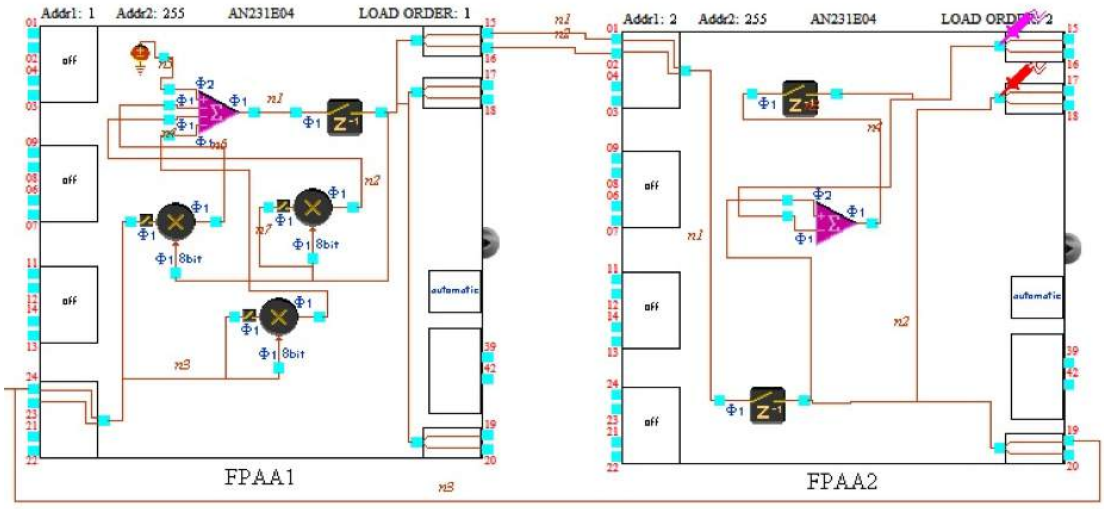


Figure 5: The circuit of nahrain discrete chaotic system using FPAA

A. *Simulation Results*

To verify the chaotic behavior and randomness properties of Nahrain system, a simulation model for the system using MATLAB is implemented. The numerical and statistical tests mentioned in section 4 are applied accordingly. This section presents first the results of chaotic behavior test, then the results of randomness test. Finally, it presents the model used for testing the synchronization of Nahrain system and its corresponding results.

B. *Results of Chaotic Behavior Tests*

After implementing 0-1 test to the Nahrain map, the following results of asymptotic growth rate K for different system variables are obtained: Kx = 0.9864, Ky = 0.9866, Kz = 0.9856. According to the results of this test, since all system

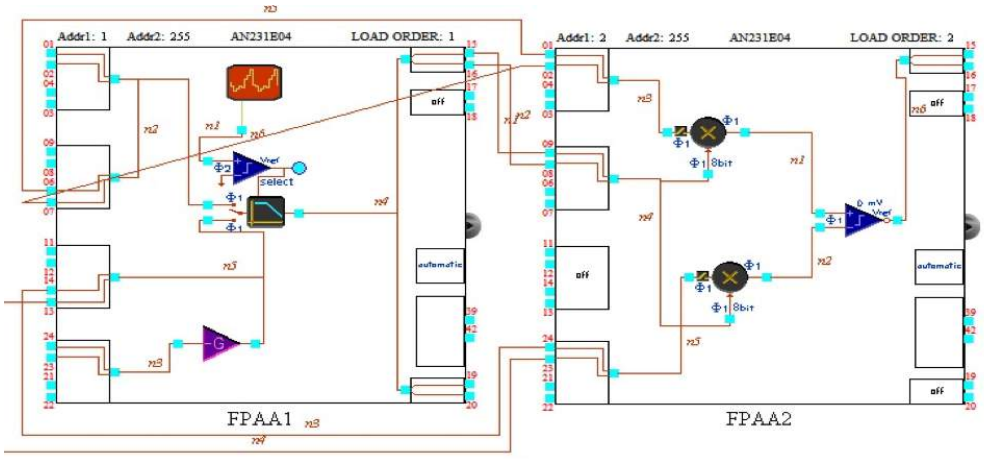


Figure 6: FPAA implementation of modulation and demodulation circuits based on nahrain discrete chaotic system

TABLE I
CONFIGURABLE ANALOG MODEL OF FPAA OF NAHRAIN DISCRETE CHAOTIC SYSTEM

FPAA1				FPAA2			
Name	**Options**	**Parameters**	**Clocks**	**Name**	**Options**	**Parameters**	**clocks**
SumDiff1 (SumDiff v1.0.1)	**Output Phase:** *Phase 1* **Input 1:** *Non-inverting* **Input 2:** *Inverting* **Input 3:** *Inverting* **Input 4:** *Inverting*	**Gain 1:** 0.5 **Gain 2:** 1.52 **Gain 3:** 1.0 **Gain 4:** 1.0	**Clock A:** *250 kHz*	**SumDiff2 (SumDiff v1.0.1)**	**Output Phase:** *Phase 1* **Input 1:** *Non-inverting* **Input 2:** *Inverting* **Input 3:** *Off* **Input 4:** *Off*	**Gain 1:** 1.0 **Gain 2:** 0.05	**Clock A:** *250 kHz*
Hold1 (Hold v1.0.2)	**Input Sampling Phase:** *Phase 1*		**Clock A:** *250 kHz*	**Hold1 (Hold v1.0.2)**	**Input Sampling Phase:** *Phase 1*		**Clock A:** *250 kHz*
Voltage1 (Voltage v1.0.1)	**Polarity:** *Positive (+2V)*			**Hold2 (Hold v1.0.2)**	**Input Sampling Phase:** *Phase 1*		**Clock A:** *250 kHz*
Multiplier1 (Multiplier v1.0.2)	**Sample and Hold:** *Input X*	**Multiplication Factor:** *1.00*	**Clock A:** *250 kHz* **Clock B:** *4 MHz*				
Multiplier2 (Multiplier v1.0.2)	**Sample and Hold:** *Input X*	**Multiplication Factor:** *1.00*	**Clock A:** *250 kHz*				
Multiplier3 (Multiplier v1.0.2)	**Sample and Hold:** *Input X*	**Multiplication Factor:** *1.00*	**Clock B:** *4 MHz*				

variables produces numbers very closed to 1 then it is a chaotic system and the chaotic behavior can be obtained from anyone of its outputs.

TABLE II
CONFIGURABLE ANALOG MODEL OF FPAA OF MODULATION AND DEMODULATION CIRCUITS

FPAA1				FPAA2			
Name	Options	Parameters	Clocks	Name	Options	Parameters	clocks
GainSwitch1 (GainSwitch v1.1.1) 	**Output Phase:** *Phase 1* **Input 1:** *Non-inverting* **Input 2:** *Inverting* **Input 3:** *Inverting* **Input 4:** *Inverting*	**Gain 1:** 0.5 **Gain 2:** 1.52 **Gain 3:** 1.0 **Gain 4:** 1.0	**Clock A:** *250 kHz*	Multiplier1 (Multiplier v1.(	**Sample and Hold:** *Input X*	**Multiplicati on Factor:** *1.00*	**Clock A:** *250 kHz* **Clock B:** *4 MHz*
PeriodicWave1 (PeriodicWave v1.0.3) 	**Output Phase:** *Phase 1* *Output Hold: on Dual Waveforms: Off Reset: Off*	**Counter Reset :**255 **Value**: *(0.977 kHz)*	**Clock A:** *250 kHz* **Clock B:** *4 MHz*	Multiplier2 (Multiplier v1 	**Sample and Hold:** *Input X*	**Multiplicati on Factor:** *1.00*	**Clock A:** *250 kHz*
GainInv1 (GainInv v1.0.1) 		Gain: 1.00	**Clock A:** *250 kHz*	Comparator1 (Comparator v1.1.1) 	**Compare to:** *Dual Input* **Input Sampling:** *Phase 1* **Output Polarity:** *Inverted* **Hysteresis**: *0mV* **Output Synch:** *None*		**Clock A:** *250 kHz*

C. Results of Randomness Test

In this wok, we used a proposed method to convert a chaotic sequences into binary ones as shown Fig.7. The conversion is based on comparing the outputs of two identical Nahrain chaotic maps running simultaneously with the same parameters (a=1.52 and b=0.05) but with different initial conditions. The initial conditions for the first map are X1(0)=0.3, Y1(0)=0.2 and Z1(0)=0.1 while for the second map they are X2(0)=0.2, Y2(0)=0.1 and Z2(0)=0.2. The output binary sequences g1, g2 and g3 are generated by comparing the outputs of the two maps on sample by sample basis according to the following equations:

$$g1(X1,X2) = \{ \begin{matrix} 1\ if\ X1 > X2 \\ 0\ if\ X1 \leq X2 \end{matrix} \} where X_1(0) \neq X_2(0) \tag{10}$$

$$g2(Y1,Y2) = \{ \begin{matrix} 1\ if\ Y1 > Y2 \\ 0\ if\ Y1 \leq Y2 \end{matrix} \} where Y_1(0) \neq Y_2(0) \tag{11}$$

$$g3(Z1,Z2) = \{ \begin{matrix} 1\ if\ Z1 > Z2 \\ 0\ if\ Z1 \leq Z2 \end{matrix} \} where Z_1(0) \neq Z_2(0) \tag{12}$$

Next a sequence of 15,000 consecutive bits of each output from the system is subjected to the tests mentioned in section 3 individually. The tests results are given in Table III. From the results in this table, we can see that the P-value of all the generated binary sequences are much higher than 0.01 which means the system is random. It can also be seen that the randomness level of output X is the best among other outputs of the system.

D. Hardware Test Results

The experimental setup of the proposed chaotic communication system using FPAA AN231K04 development board is shown in Fig.8. The hardware test results are divided into two parts: the result of Nahrain chaotic System implementation

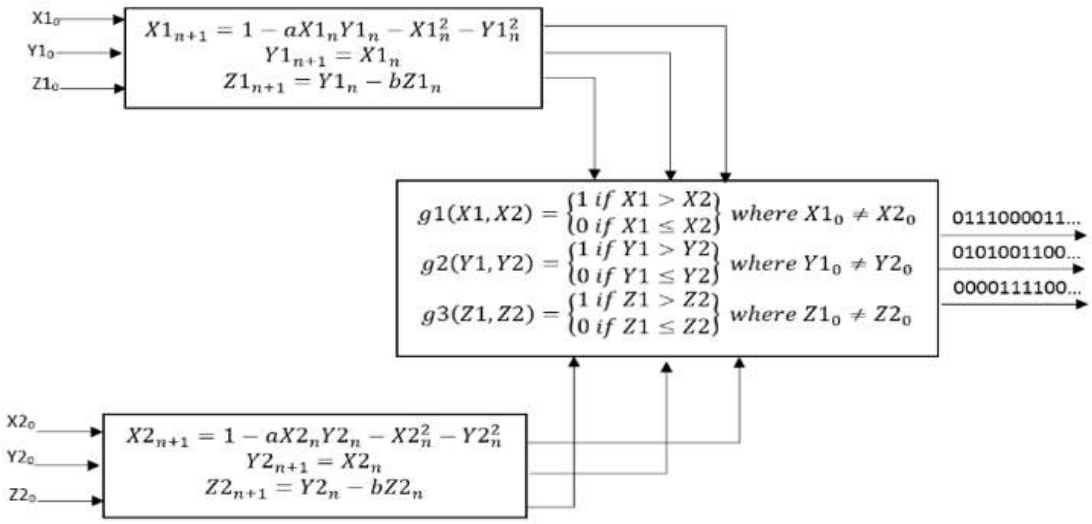


Figure 7: Random Bit generator

TABLE III
THE RESULTS OF THE RANDOMNESS TESTS

Test	X	Y	Z	*P-value >= (0.01-0.001)*
Frequency (MonoBit) Test	0.5787	0.5787	0.2739	accept
Frequency (Block =1000) Test	0.5031	0.5168	0.8993	accept
Run Test	0.5917	0.5917	0.2855	accept
Longest Run of Ones in a Block (128)	0.9931	0.9997	0.9606	accept
Binary Matrix Rank Test	0.2030	0.2030	0.0433	accept
DFT Test	0.4118	0.3049	0.4118	accept
Maurer's Test	0.8604	0.8744	0.8670	accept
Approximate Entropy Test	0.4002	0.4002	0.5458	accept
Cumulative Sum Test	0.9767	0.9767	0.5458	accept
Random Excursions Test	0.1085	0.1085	0.0253	accept
Random Excursions Variant Test	0.8808	0.8814	0.9042	accept

and the results of chaotic modulation/demodulation implementation.

E. Hardware Result of Nahrain Chaotic System Implementation

To observe the behavior of the Nahrain chaotic map, the FPAA model is downloaded to the development board by setting the parameters in Eq.1. as follows: a=1.52 and b=0.05. The experimental results of the FPAA realization are measured via an oscilloscope in time domain of the state-variables of the system namely X, Y and Z as shown in Fig.9. The chaotic attractor illustration produced by experimental realization of the system are shown in Fig.10. These figures show that the programmable hardware testing results very match to the simulation results of system that shown in Fig.3. Table IV illustrates the power consumptions, CAB usage capacity and clock frequency of these implementations. Fig.10 show that the chaotic attractors are strange with good state space, so they can be used for generating secure key for multimedia encryption and can be used as carrier wave for secure multimedia transmission.

TABLE IV
THE HARDWARE RESOURCES OF THE FPAA IMPLEMENTATION OF NAHRAIN CHAOTIC SYSTEM

	FPAA1	FPAA2
Power consumption	165 50 mW	74 22 mW
CAB1(used/total capacity)	7/8	5/8
CAB2(used/total capacity)	6/8	2/8
CAB3(used/total capacity)	6/8	0/8
CAB4(used/total capacity)	6/8	0/8
Clock Frequency (used/ Maximum Allowed)	250kHz,4MHz/4MHz	250kHz/4MHz

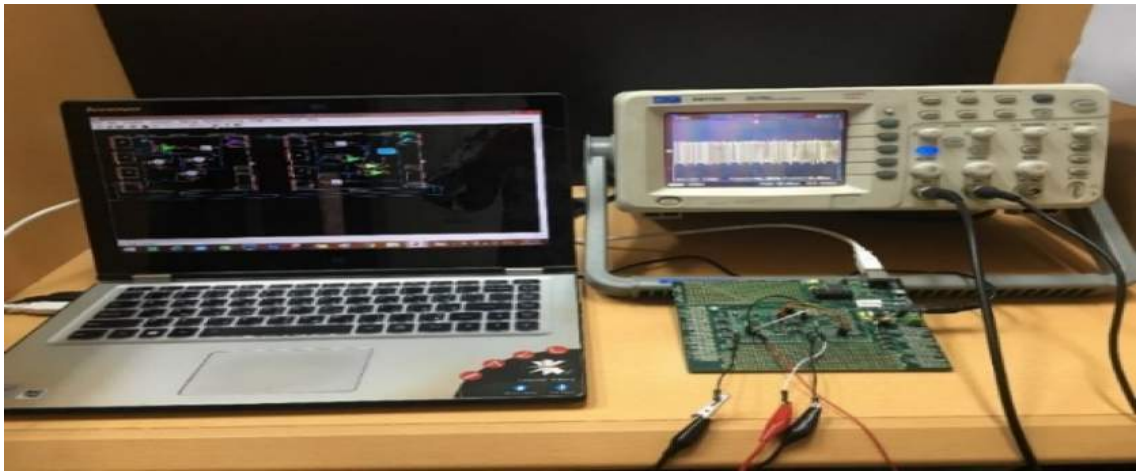


Figure 8: The experimental setup of the proposed hardware platform

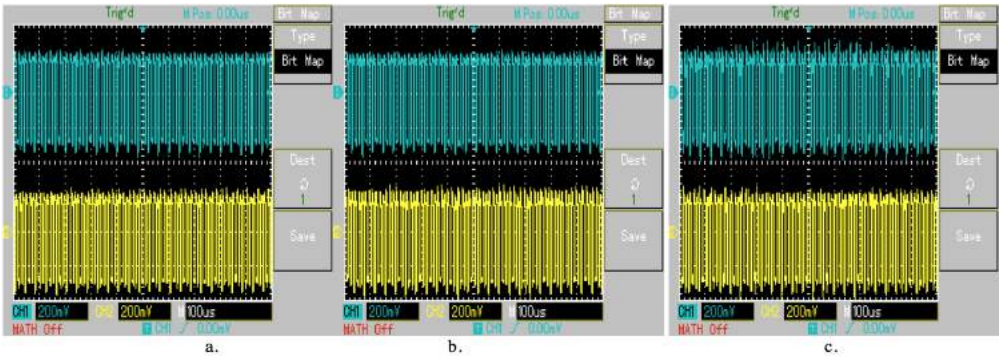


Figure 9: Experimental realization of state-variables a. X and Y b. X and Z c. Y and Z

F. Hardware Results of Chaotic Modulation and Demodulation

To observe the behavior of the modulation and demodulation method, the FPAA model is downloaded to the development board. The experimental results of the FPAA realization are measured via an oscilloscope in time domain of the carrier X chaotic signal and modulated signal as shown in Fig.11.a. The recovered and modulated signals produced by experimental realization of the system are shown in Fig. 11.b-d. These figures show that the modulated signals are random like noise and

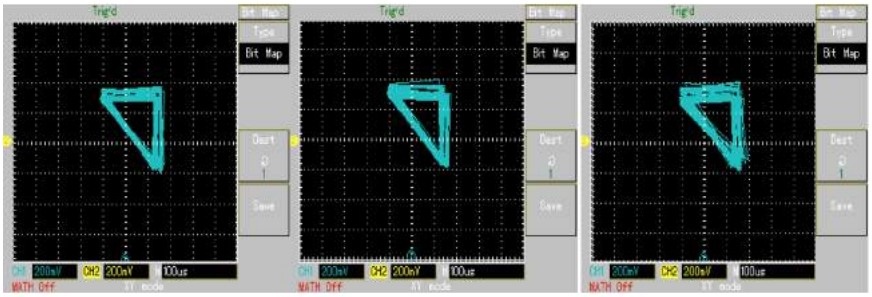


Figure 10: Experimental realization of chaotic attractor: a. X-Y attractor, b. X-Z c. attractor Z-Y attractor

the attacker cannot extract any useful information from these transmitted signal. So FPAA-based chaos added a significant reliability to the proposed secure transmission system. Table V illustrates the power consumptions, CAB usage capacity and clock frequency of these implementations.

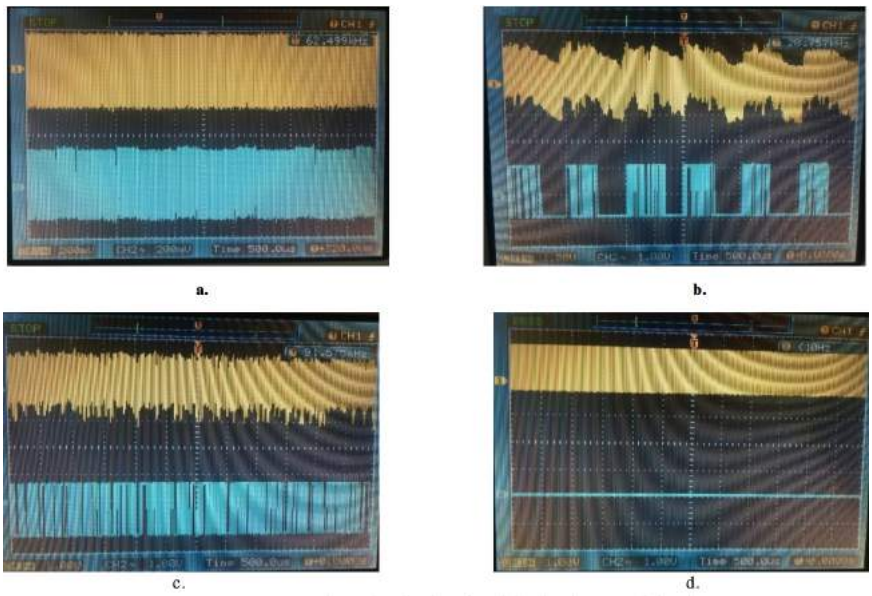
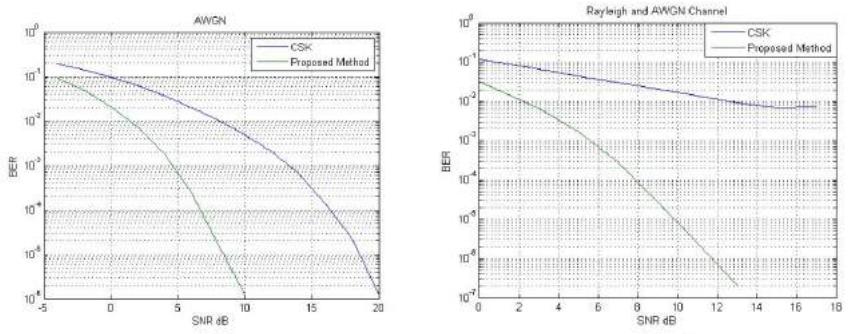


Figure 11: Experimental realization of modulated and recovered signal a. Experimental realization of carrier and modulated signal, b. Data size 256 bit stream of 128 bit of ones and 128 bit of zeros. c.Data size 256 bit stream of zeros. d.Data size 256 bit stream of ones

To evaluate the performance of the proposed modulation methods in noisy channel, many simulation tests have been done.Figure 12 show the Bit Error Rate (BER) curves for proposed types of modulation method over AWGN and fading channel. In Fig.2. The BER curves obtained for traditional CSK and proposed modulation method by using Nahrain chaotic systems as a carrier. The proposed modulation methods show better performance than traditional CSK, where the proposed modulation methods recover the data with zero BER at 10 dB.

TABLE V
HARDWARE RESOURCES OF FPAA IMPLEMENTATION OF MODULATOR/DEMODULATOR

	FPAA1	FPAA2
Power consumption	75 23 mW	95 28 mW
CAB1(used/total capacity)	8/8	6/8
CAB2(used/total capacity)	4/8	6/8
CAB3(used/total capacity)	0/8	0/8
CAB4(used/total capacity)	0/8	0/8
Clock Frequency (used/ Maximum Allowed)	250kHz,4MHz/4MHz	250kHz/4MHz



a. Transmission over AWGNG channel b. Transmission over Rayleigh with AWGN Channel

Figure 12: BER curves obtained for proposed modulation method

VII. CONCLUSION

The implementation of a chaotic system based on FPAA programmable hardware is very convenient for reconfigurable design based in its nonlinear structure. FPAA offer multiple advantages that exceed the advantages offered by the other electronic components, in reducing the time taken in designing the different analog circuits; in addition to the possibility of reforming the different circuits for the purpose of getting a design of high reliability. The simulation results of system very match to the programmable hardware results. The experimental results of the FPAA realization show that the modulated signals are random like noise and the attacker cannot extract any useful information from these transmitted signal. The BER curves obtained the proposed modulation methods show better performance than traditional CSK, where the proposed modulation methods recover the data with zero BER at 10 dB. FPAA-based chaos added a significant reliability to the proposed secure transmission system. This system can be used efficiently as a programmable chaos generator in plentiful chaos-based applications. Since a FPAA device can be used in state of roughly all electronic hardware for implementations of discrete chaotic system, this programmable and reconfigurable implementation offers more dynamic, modest and economic solutions. FPAA very sensitive to high temperature and requires medium temperature environment. Because this type implementations provide the potential of resilient and reconfigurable design of many analog chaotic systems based on mathematical design without requirement to complex electronic hardware, FPAA-based chaos studies will be very valuable for the researchers from different science and engineering fields.

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