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HARDWARE IMPLEMENTATION OF DCSK COMMUNICATION SYSTEM USING XILINX SYSTEM GENERATOR

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Abstract: In this paper, the implementation of the non-coherent differential chaos shift-keying (DCSK) system over AWGN channel with different spread factor using Xilinx System Generator (XSG) are proposed. Using XSG because it is more reliable and flexible and easy to update and modify the design system in addition to gives the perfect design for FPGA technicality for hardware design compared with the conventional FPGA design. The hardware co-simulation of the DCSK system is performed on the SP605 xc6slx45t-3fgg484 evaluation board with clock frequency 27 MHZ. The results of hardware simulation prove that the system is worked in the correct form. The system is routed in successfully using ISE 14.5 program with maximum frequency 39.587, 41.592 MHZ in modulation, and demodulation respectively. The Xilinx system generator (XSG) is most easier, flexible, and reliable and gives an optimum design for the FPGA technique comparing with conventional FPGA design.

Keywords: *Differential Chaos Shift Keying, FPGA, Xilinx System Generator, 0-1 Test, Hardware Co-simulation.*

1. Introduction

Chaos communication system [7] is a one of the most important branch in communication security systems because has a very high security, where the chaos system generates the chaotic signal, which is a random and non-periodic signal with wideband range, difficult to predict or to reconstruct and it's sensitive to initial conditions and values, therefore more security is achieved and the transmission become more difficult to be intercepted so the decoding of modulated data information is less easy [5]. Chaotic modulation communication is one of the most important scheme in wireless communications because it's characteristics including reduction of fading effects, jamming resistance and the low probability interception, this is make it suited for various spread spectrum modulation system [8]. Chaos system based wireless communication can be classified into two types, either coherent or non-coherent detection in demodulation side, which are Chaos Shift Keying (CSK) system [1,6] and Differential Chaos Shift Keying (DCSK) system [1,2,4,13]. CSK is a coherent system therefore it's needed synchronization between transmitter and receiver (needed to reproduce chaotic signal at the receiver side) and this is impossible to implement due to the high complexity at the receiver side, so the coherent detection is unpractical in fast fading channel due to their short coherence time [3]. Therefor DCSK is better than CSK because it's a non-coherent detection, so it's not needed any synchronization between transmitter and receiver sides, in which the chaotic signal is not needed to reproduce in the receiver side. Furthermore, it has a good performance over multipath fading channel,

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suitable to ultra wide band (UWB) applications and simplicity in the structure implementation make it used in many wireless communication system [1]. The main drawbacks of DCSK system is the receiver require a radio frequency (RF) delay line and when sending reference samples spent half of bit duration, which leads to low data rate and energy efficiency. So to improve performance of DCSK and make it more security, several types of DCSK are proposed to increase the data rate of DCSK, such as Reverse DCSK (RE-DCSK) system [8] was proposed for reliable and high data rate with low cost. Quadrature Chaos Shift Keying (QCSK) system [9] was proposed to double the information rate with the same bandwidth occupation at the cost of the system complexity increase. Code Shifted DCSK (CS-DCSK) system [10-11] was proposed to satisfy the demand of Ultra-Wideband (UWD) communication. Multicarrier DCSK (MC- DCSK) system [18] was proposed to enhance the spectrum efficiency and energy efficiency. Wavelet Packet Modulation(WPM) is a new multicarrier based DCSK [17] was proposed to use discrete wavelet packet transform (DWPT) which is real arithmetic instead OFDM system that uses fast Fourier transform (FFT) which is complex arithmetic to improved spectral efficiency.

In the modern communication systems, the software design replaced by the hardware design due to flexibility for adapting the hardware design. The desired system can be designed by FPGA with high speed and minimum cost. In the other words, Xilinx system Generator (XSG) tool is used to implement DCSK system because it is easier, flexible, reliable, and easy to update and modify the design system. It available different blocks of digital processing (DSP) building that exists in XSG DSP block set in Simulink tools to build a different models and generate Hardware Description Language (HDL) code for the design system. There are little studies of DCSK system using FPGA technique, in [3]. In [3] Haar Wavelet Packet Modulation (HWPM-DCSK) is realized by using FPGA technique due to flexibility and efficient design with high clock rates therefore that can be used to realize digital communication systems, where Haar WPM combine with DCSK system which is sufficient way to improve the performance of DCSK system and fast algorithm for HWPM transform was used to enhancement the complexity of the WPM system.In this paper, the DCSK system is designed using XSG tool [14] in efficient way, less cost and high speed. According to the increased complexity of FPGA, several tools, and software have been associated with FPGA to can implement the algorithms in an easy way. XSG is a plug-in to Simulink that is developed by Xilinx, where a system generator is a high-level tool that fully integrated into MATLAB Simulink to design high-performance DSP for Xilinx FPGA. XSG has a collection of libraries including operations of basic logic such as AND, OR, multiply blocks. Therefore, it is well suited for developing DSP applications. The Xilinx/MATLAB Simulink block set includes a wide range of primitive functions and more complicated signal processing applications and this makes the designers develop the algorithms easily and benefits from MATLAB property during the design and test phases. XSG available different blocks of digital processing (DSP) building that exists in the XSG DSP block set in Simulink tools to build different models and generate Hardware Description Language (HDL) code for the design system. Fixed point is used in the implementation of chaotic signal [12], this effect the characteristic of chaotic system, therefore, the test 0-1 is used to test the chaotic signal if it is a regular or chaotic signal. The comparison between the BER analytical and system generator results for different spread factor, β, is studied. Furthermore, the hardware co-simulation of DCSK system is performed on SP605 xc6slx45t-3fgg484 evaluation board with clock frequency 27 MHZ [15].

The rest of the paper is organized as: Section II introduce the architecture of DCSK communication system and Section III contains XSG based DCSK system. In Section IV the simulation results and discussion are presented, and FPGA results are presented in Section V. Finally, the conclusion is drawn in Section IV.

2. DCSK Communication System

Figure (1) shows the block diagram of transceiver DCSK system over AWGN channel. To send one bit, 2β samples are needed which is the spreading factor, where β is an integer. The transmitted sequence of DCSK modulation is given by [1]:

$$s_k = \begin{cases} X_k & for\ 1 < k \le \beta \\ d_i\, X_{k-\beta} & for\ \beta < k \le 2\beta \end{cases} \quad (1)$$

where X_k and $X_{k-\beta}$ are the reference chaotic sequence and its delay version respectively which is generated using the second order Chebyshev polynomial function (CPF) according to [3]

$$X_{k+1} = 1 - 2X_k^2 \quad (2)$$

The DCSK modulated signal is passed through additive white Gaussian noise (AWGN) channel ,n_k, with zero mean and variance $N_0/2$ to produce the received signal $r_k = s_k + \sigma\, n_k$,where σ is the standard deviation of the noise power. To detect the original sending bits, the received reference sequence, r_k ,$k \in [0, \beta)$, is correlated with the received information sequence, $r_{k-\beta}$, $k \in [0, \beta)$ to produce the *i*-th correlator output, C_i [1],

$$C_i = \sum_{k=1}^{\beta} r_k . r_{k-\beta} \quad (3)$$

Then the output detector is comparing with zero threshold to recover the *i*-th information bits, $\tilde{d}_i$.

The BER analytic of DCSK system under AWGN channel is derived in [1] and can be expressed in terms of β and energy per bit to noise ratio (E_b/N_0), where E_b is the energy per bits that is calculated as $E_b = 2\sum_{k=1}^{\beta} X_k^2$, as [1]:

$$\mathrm{BER_{DCSK}} = \frac{1}{2} erfc\left(\left(\frac{4}{E_b/N_0} + \frac{2\beta}{(E_b/N_0)^2}\right)^{-\frac{1}{2}}\right) \quad (4)$$

where *erfc* is the complementary error function.

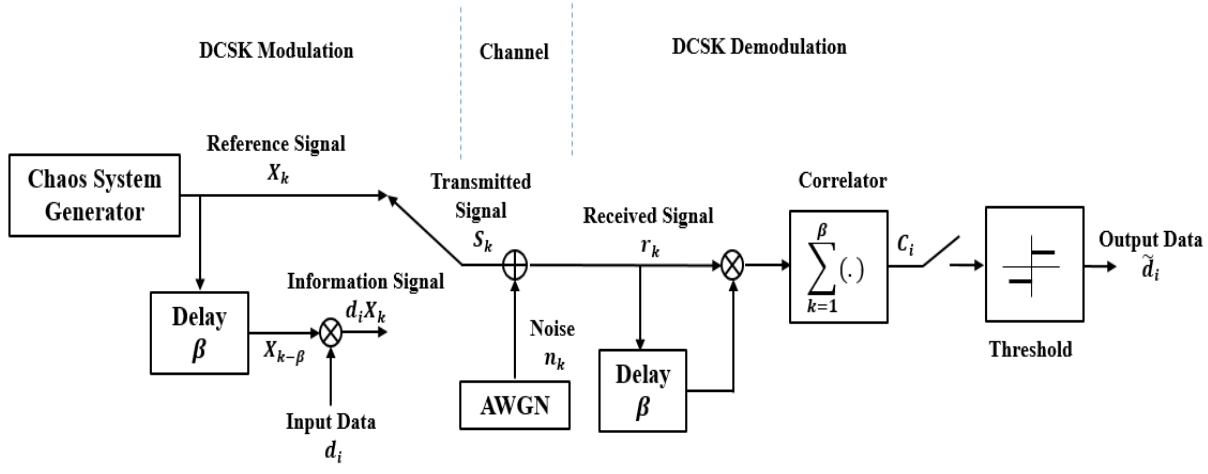

Figure 1. Block diagram of DCSK communication

3. XSG Based DCSK Communication System

Figure (2) shows the XSG block diagram of DCSK communication system. Five main components are presented in this figure that are source input, DCSK modulation, AWGN channel, DCSK demodulation and BER calculation. The source input is generated using Bernoulli Binary generator function that is Simulink/MATLAP (SM) function which generates binary stream sequence. Gateway In and Gateway out are system generator function used to convert from SM to System Generator (SG) and from SG to SM environment respectively. The detail description components of DCSK modulation, AWGN channel and DCSK demodulation, which are SG components, are presented below.

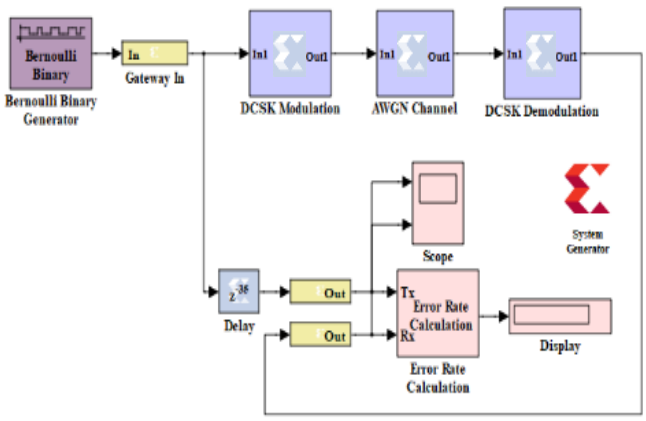

Figure 2. Implementation of DCSK system by Xilinx System Generator (XSG)

3.1. DCSK Modulation System

The structure of DCSK modulation is illustrated in Figure (3). In the first, the chaos system generator is used to generate the chaotic signal, this signal represents the reference of the system. Figure (3) shows XSG block diagram of chaos system generator function. This function is implemented according to Equation (2). The control initial function is used to select the initial value in the first cycle and it is value equal to one and then becomes zero value to allow the feedback values of x_k to enter the system. This function is implemented in Figure (4) using one register with initial value one and one XOR logic function with itself value. The output of XOR is feedback to the register to make control initial always zero for the rest of cycles.

In the next step the chaotic signal is passed through a delay of β samples (β =32 here) and multiply it by data input to produce the information sequence. The data bits are generated by Bernoulli binary generator SM function to produce the stream bits with sample time greater than chip time by 2β factor (here 2×32 =64).

After that, the reference and information signals are time multiplexed using Multiplexer XSG block to produce the transmitted signal. In multiplexer, the Counter and Slice XSG block are used as the selector to passes the reference signal in the first 32 samples and after 32 samples the information signal. The parameter setting of Counter and Slice are: for Counter, initial value =0, number of bits= $\log_2(2\beta)$=6, and for Slice, no. of bits=1, relative to MSB (select binary lower bit location). When the output of selector is (0) d_o is selected and the output is taking from reference signal that is continuous to 32 samples and after the 32 samples the output of selector become (1) and the output of multiplexer is switched to d_1 to output the information signal that is continues up to 32 samples and so on.

At the receiver side, the transmitted signal is added with the additive white Gaussian noise (AWGN) as shown in Figure (3). The AWGN function is depicted in Figure (6), where the noise signal is generated using White Gaussian Noise Generator block and the output is multiplied by the standard deviation of the noise power (σ) that is related to the Signal to Noise Ratio (SNR).

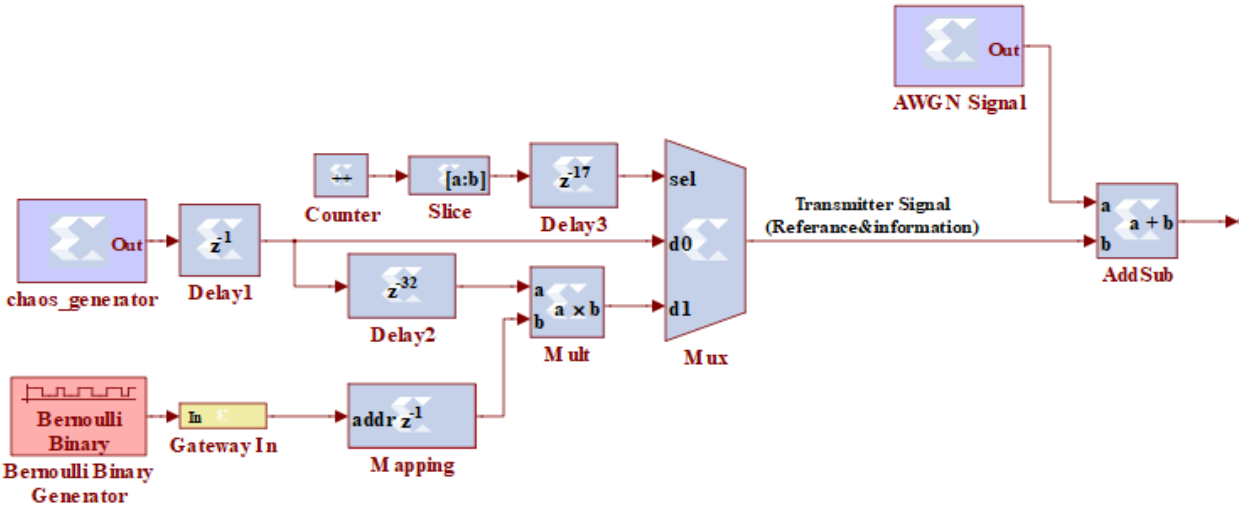

Figure 3. XSG block diagram of DCSK Modulation System with the AWGN Channel.

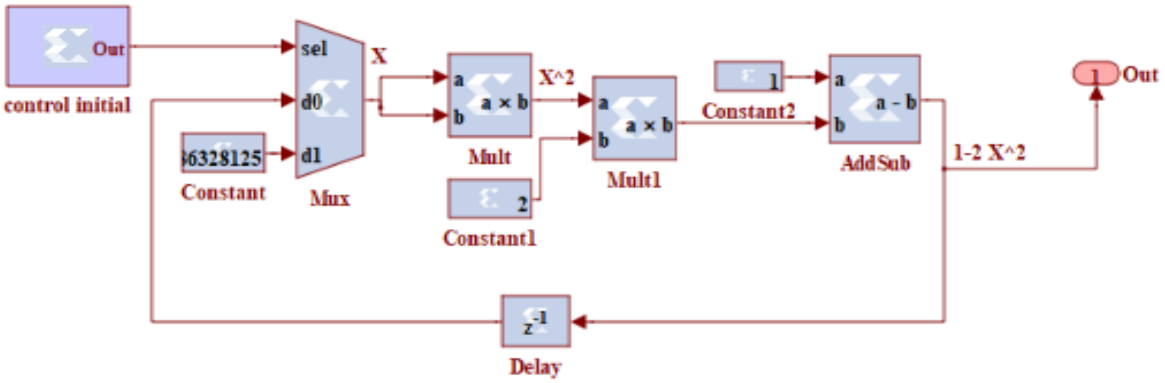

Figure 4. XSG block diagram of Chaos System Generator

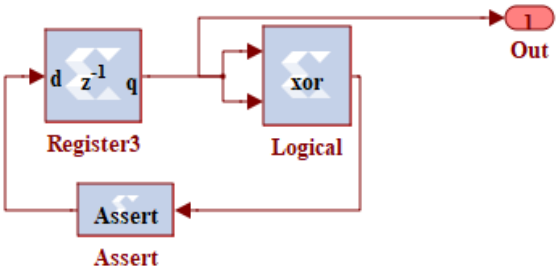

Figure 5. XSG block diagram of Control Initial

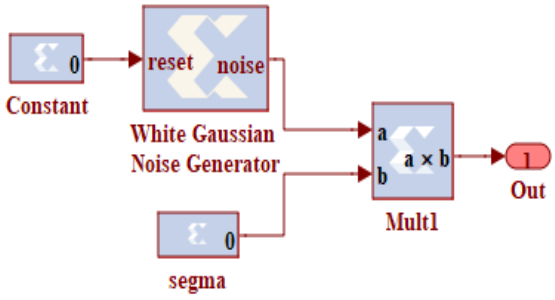

Figure 6. XSG block diagram of AWGN channel

3.2. DCSK Demodulation

In DCSK demodulation, the serial received sequence is converted to parallel samples using serial to parallel convertor block, this converter is not available in Simulink library and can be implemented by using the delays and shift registers (here for β=32, using 64 delays & 64 shift register). The output is parallel samples with 64 samples that are entered to the correlator function which is a correlation between the information sequence with the reference sequence. It is performed from multiplier and add-sub blocks The final step the correlator output is passing through threshold block, where the signal is comparing with zero value to recover the binary data, i.e. if the output correlator signal is greater than zero the output of threshold becomes one. Enable of threshold becomes one after a delay specify according to reach the first sample of output signal of correlator.

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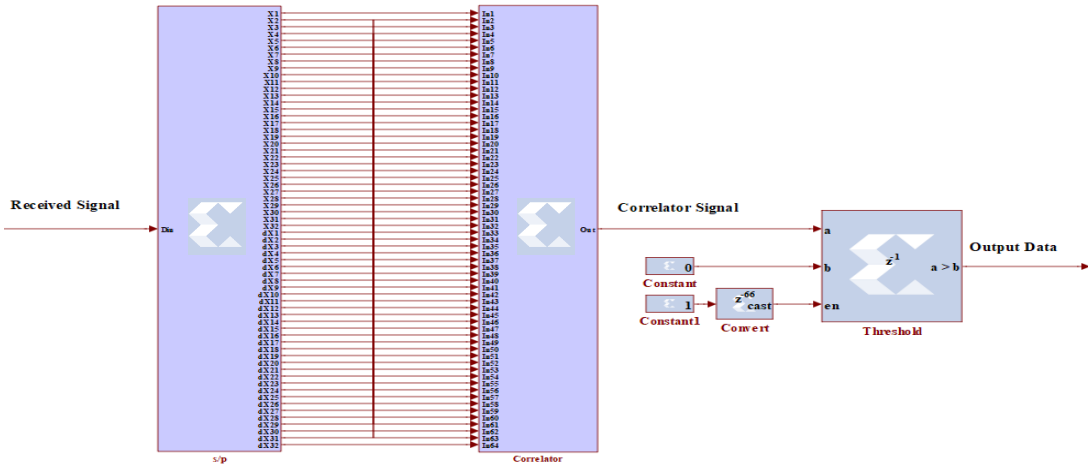


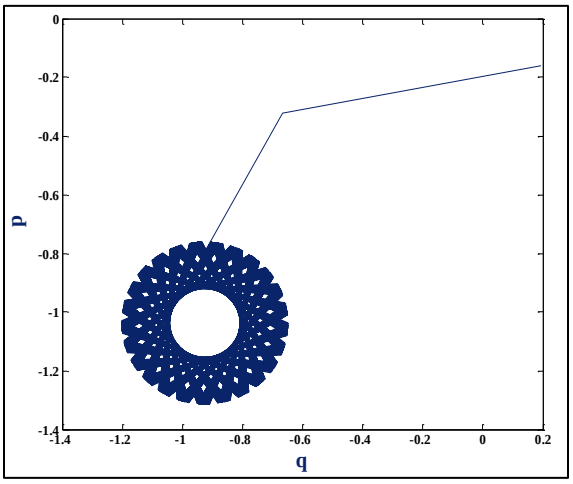
Figure 7. XSG block diagram of DCSK Demodulation system

4. Simulation Results

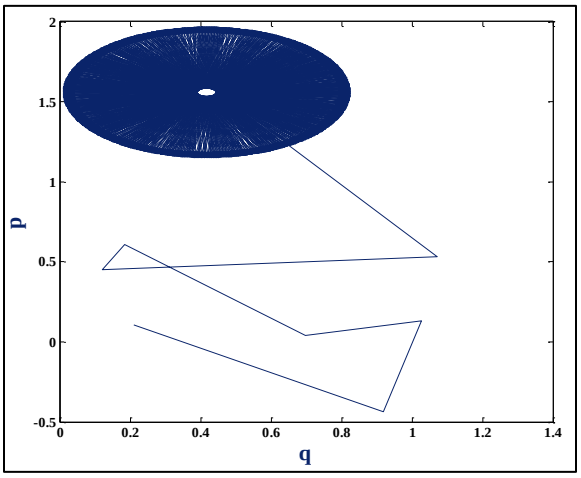
In the first, to determine the chaotic system behavior if it is generated a chaotic or regular sequence, the 0-1 Test [16] is established. In this method when the output is 1, the chaos behavior is achieved, or it is a non-chaotic for 0. Using the 0-1 test over calculating the LE method because of can be used in time series data and in both discrete and continues systems. By taking different values of word length (WL) in range (8-32) bits and make integer length (IL) equal to 3, therefore the fractional length (FL) =WL-3. In other words, WL = IL + FL and the output type is fixed point with signed (2'comp). Table (1) shows the relation between fixed point length and 0-1 Test to classify if the chaotic sequence generator is chaotic or regular depends on the test. Figure (9) shows p-q characteristic of 0-1 test versus different fixed point format.

Table (1). effect of fixed point format on 0-1 Test.

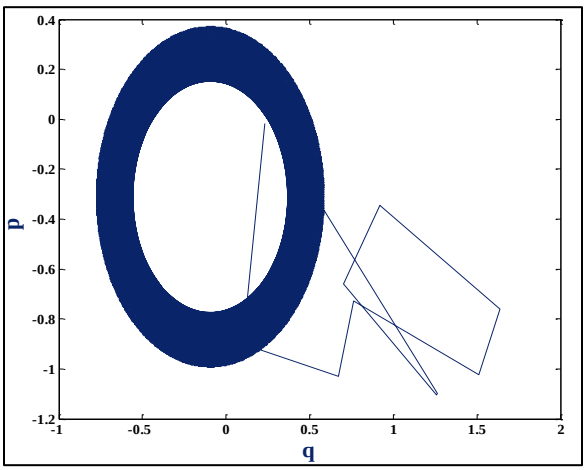
Word length (WL)	Fraction length (FL)	0-1 Test
8	5	0.2569
10	7	-0.0062
14	11	0.1664
18	15	0.76
20	17	0.9960
22	19	0.9973
26	23	0.9988
30	27	0.9986
32	29	0.9987



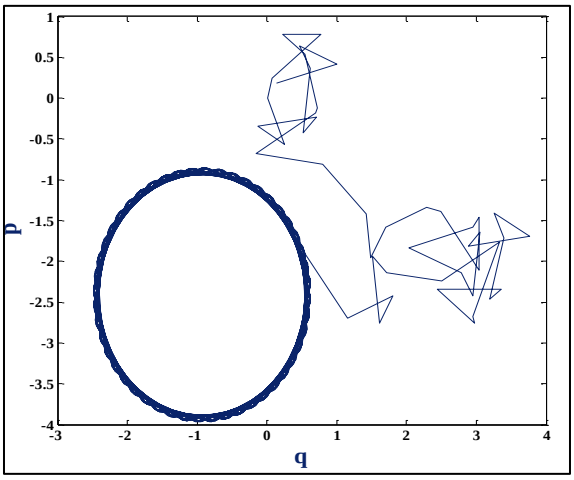
(a) Regular dynamics for WL=8, FL=5



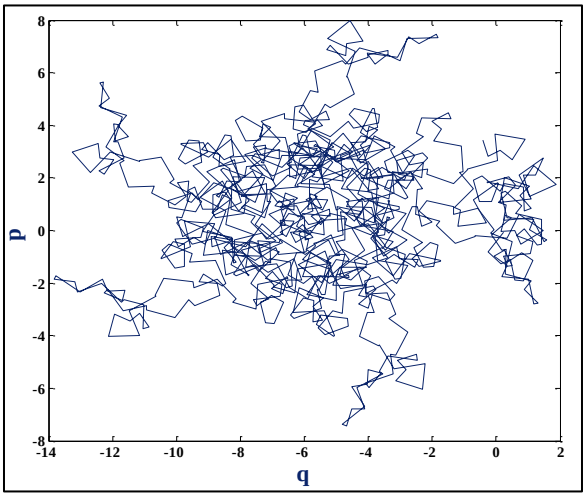
(b) Regular dynamics for WL=10, FL=7



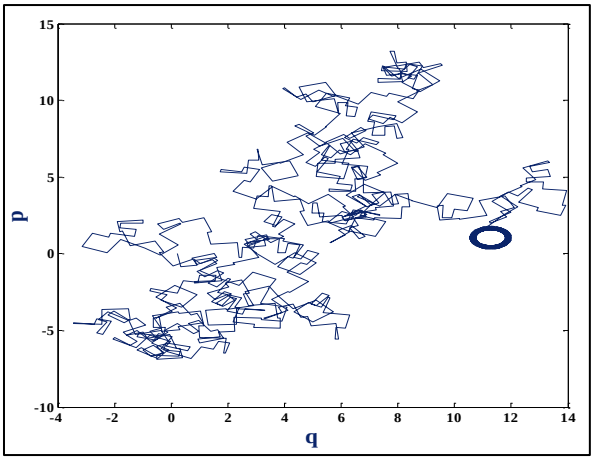
(c) Regular dynamics for WL=14, FL=11



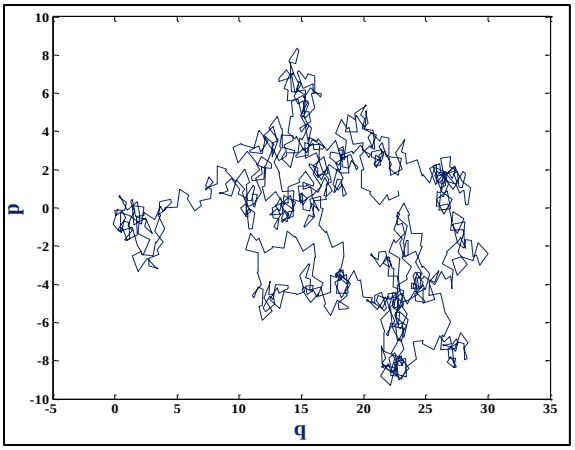
(d) Regular dynamics for WL=18, FL=15



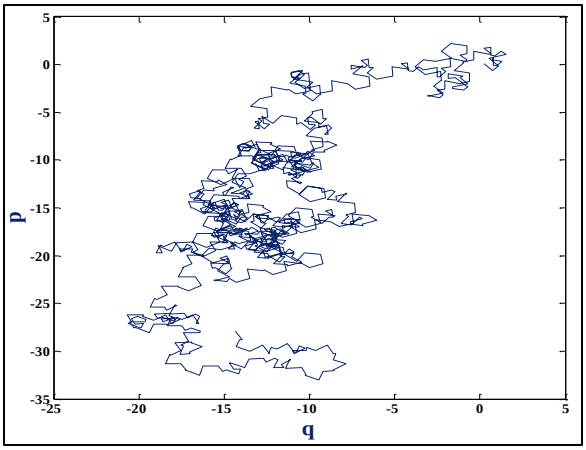
(e) chaotic dynamics for WL=20, FL=17



(f) chaotic dynamics for WL=22, FL=19



(g) chaotic dynamics for WL=26, FL=23



(h) chaotic dynamics for WL=30, FL=27

Figure 8. illustration of the system behavior by using 0-1 Test for different fixed-point length. (a) For WL=8, FL=5. (b) For WL=10, FL=7. (c) For WL=14, FL=11. (d) For WL=18, FL=15. (e) For WL=20, FL=17. (f) For WL=22, FL=19. (g) For WL=26, FL=23. (h) For WL=30, FL=27.

Figure (9) and (10) illustrate the time waveforms of DCSK modulation side for β=32. Figure (11) shows the serial to parallel converter at the receiver side. Figure (12) illustrates the correlator waveform and detection stream bits. Figure (13) shows the comparison between the input data bit and detected stream bits.

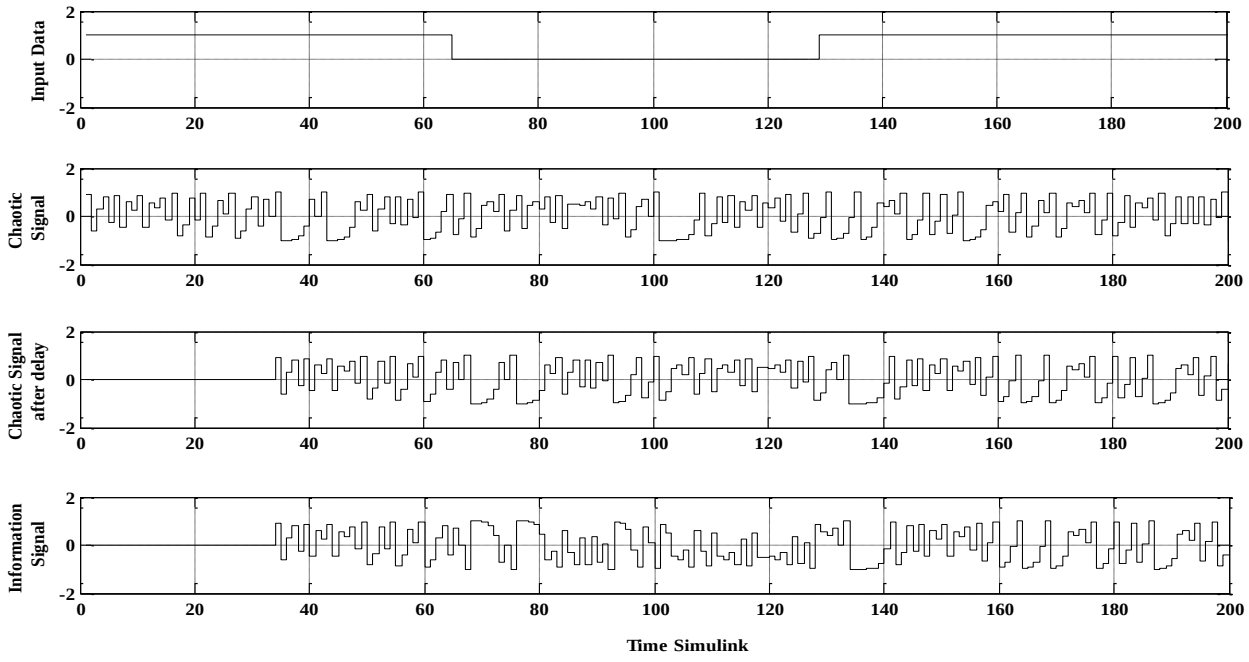


Figure 9. XSG waveform simulation of input data and chaotic signals of DCSK system

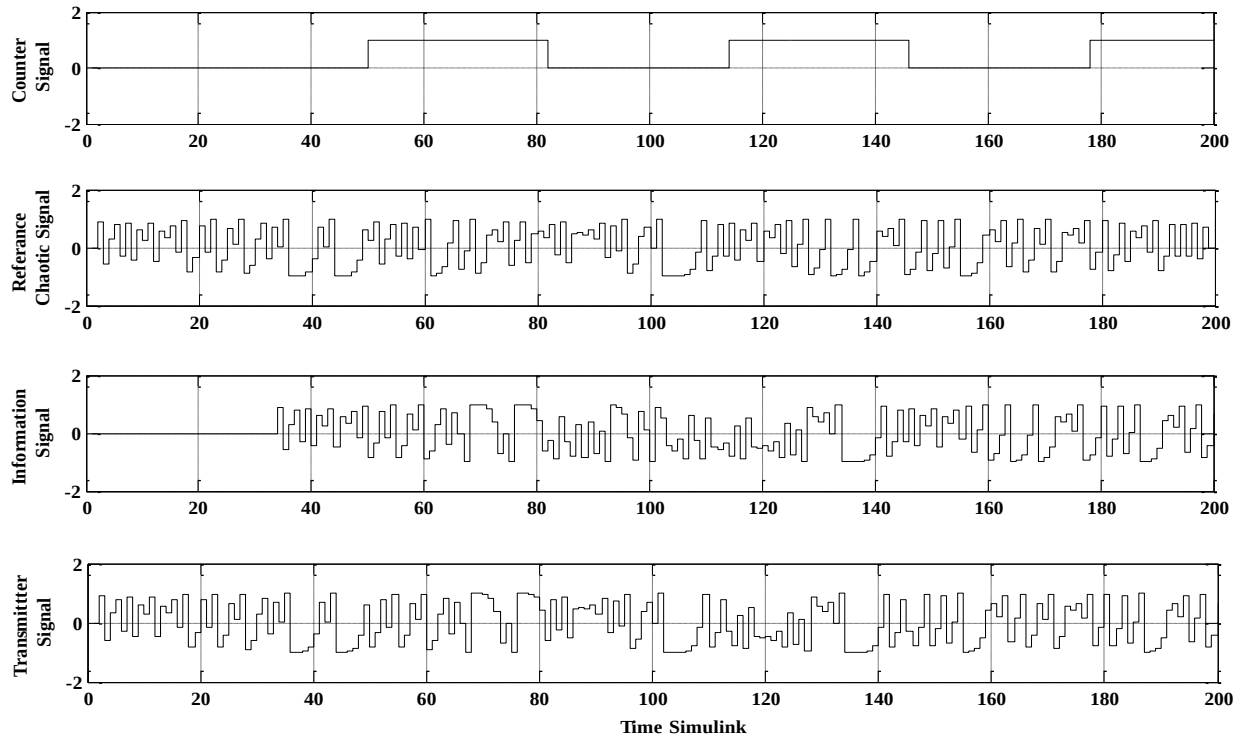


Figure 10. XSG waveforms simulation of modulation DCSK system (Reference & Information signals)

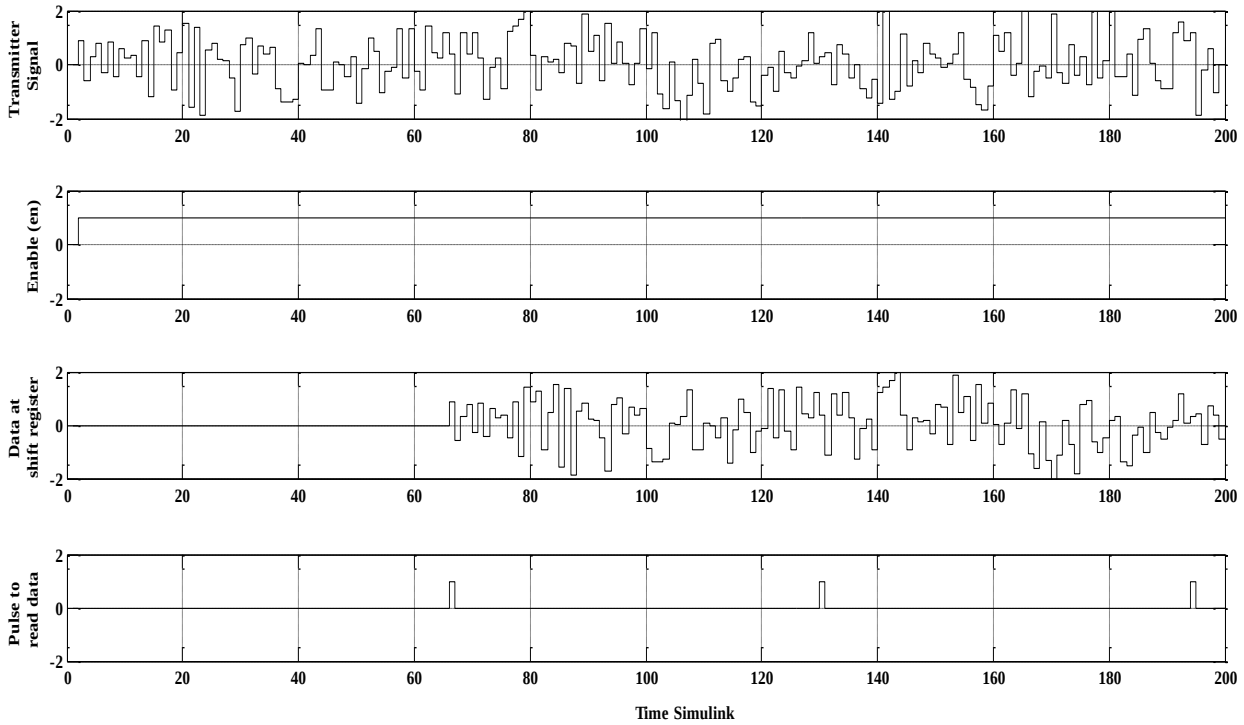


Figure 11. XSG waveform simulation of serial to parallel block

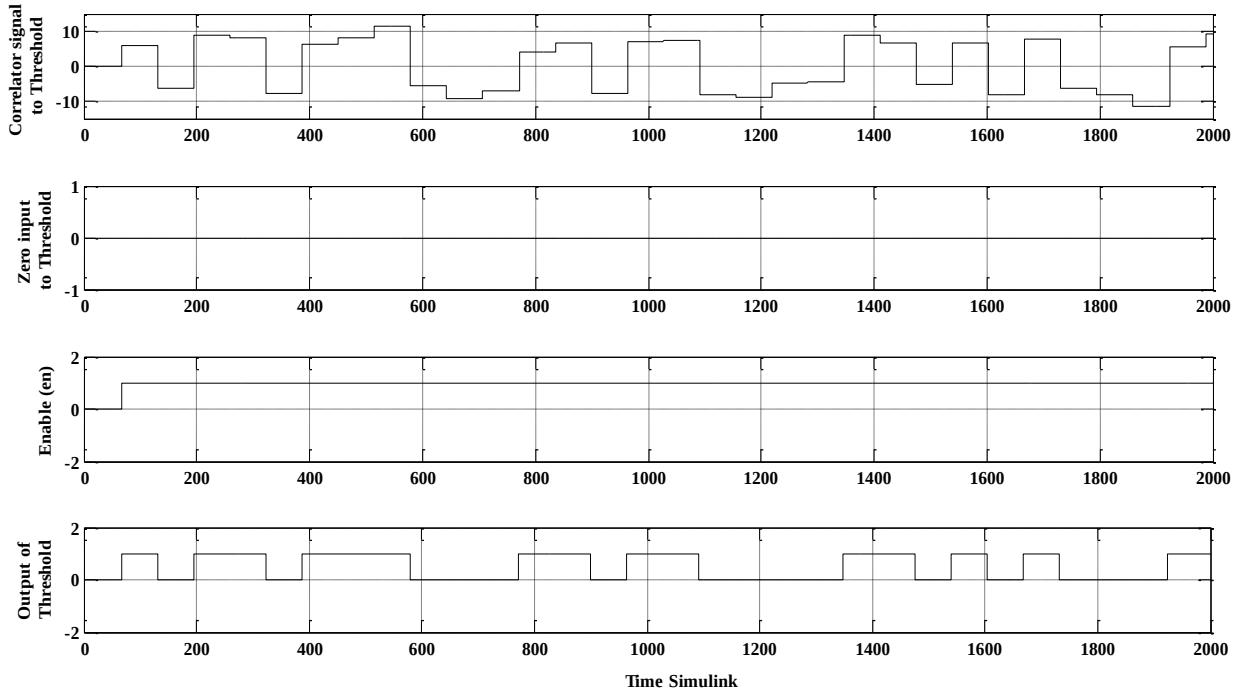


Figure 12. XSG waveform simulation of correlation output

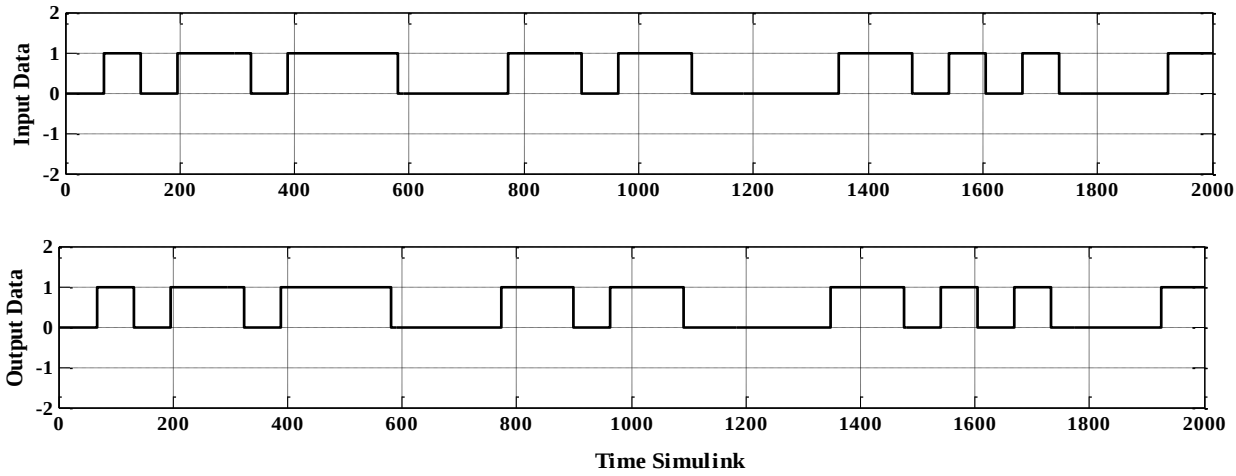


Figure 13. XSG waveform simulation of input & output data of DCSK system

Tables (2)-(5) show the Comparison between BER Theory and BER System Generator under AWGN channel for β =4,8, 16 and 32 respectively. The standard deviation of the noise, σ, is also considered in these tables for every E_b/N_0 value. Figures (15-18) plot the BER comparison between the analytic and system generator results versus SNR values.

Table 2. The Comparison between BER Theory and BER SG under AWGN channel versus E_b/N_0 at β =4

E_b/N_0 [dB]	σ	BER Theory	BER SG
0	*1.3976*	*0.3415*	*0.3558*
1	*1.2456*	*0.3110*	*0.3145*
2	*1.1102*	*0.277*	*0.2797*
3	*0.9894*	*0.2401*	*0.2388*
4	*0.8818*	*0.2015*	*0.1813*
5	*0.7859*	*0.1625*	*0.1383*
6	*0.7005*	*0.1249*	*0.1013*
7	*0.6243*	*0.0904*	*0.0664*
8	*0.5564*	*0.0608*	*0.05279*
9	*0.4959*	*0.0374*	*0.03039*
10	*0.442*	*0.0206*	*0.0192*
11	*0.3939*	*0.0099*	*0.009988*
12	*0.3511*	*0.004*	*0.005332*
13	*0.3129*	*0.0013*	*0.0016*
14	*0.2789*	*0.0013*	*0*
15	0.2485	0.0003	0
16	0.2215	0.0001	0
17	0.1974	0	0
18	0.176	0	0
19	0.1568	0	0
20	0.1398	0	0

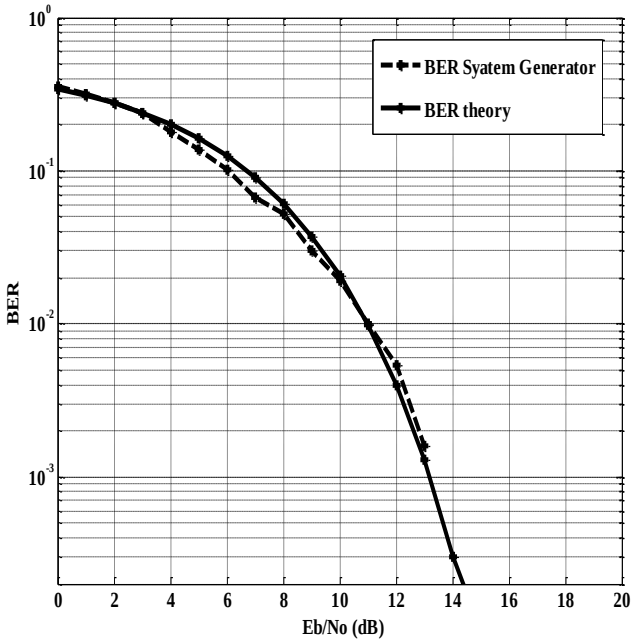


Figure 14. BER comparison of DCSK system between theory and SG results for $\beta = 4$.

Table 3. The Comparison between BER Theory and BER SG under AWGN channel versus E_b/N_0 at β =8.

E_b/N_0 [dB]	σ	BER Theory	BER SG
0	*1.9765*	*0.3759*	*0.3758*
1	*1.7616*	*0.3489*	*0.3518*
2	*1.57*	*0.3177*	*0.3037*
3	*1.3993*	*0.2822*	*0.2959*
4	*1.2471*	*0.2432*	*0.2311*
5	*1.1115*	*0.2017*	*0.1927*
6	*0.9906*	*0.1595*	*0.1519*
7	*0.8829*	*0.1189*	*0.1199*
8	*0.7869*	*0.0823*	*0.07677*
9	*0.7013*	*0.0521*	*0.04478*
10	*0.6250*	*0.0294*	*0.02666*
11	*0.5571*	*0.0144*	*0.02285*
12	*0.4965*	*0.0059*	*0.003199*
13	*0.4425*	*0.002*	*0.003199*
14	0.3944	*0.0005*	*0*
15	0.3515	0.0001	0
16	0.3133	0	0
17	0.2792	0	0
18	0.2488	0	0
19	0.2218	0	0
20	*0.1977*	0	0

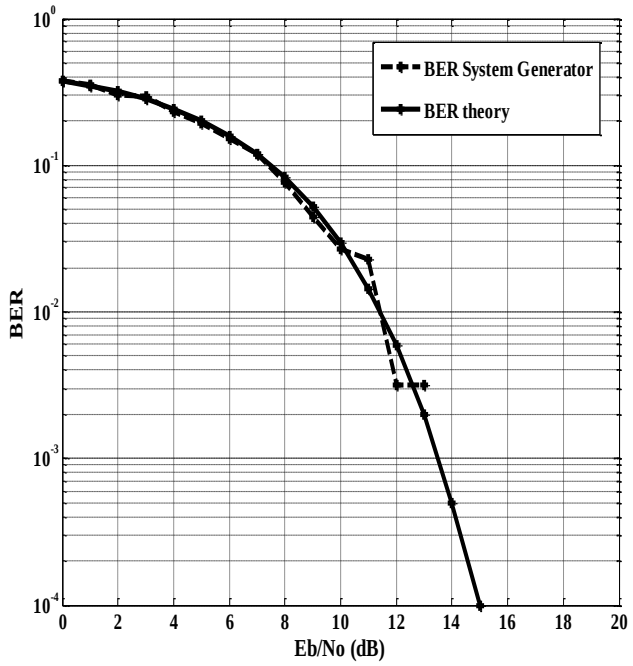


Figure 15. BER comparison of DCSK system between theory and SG results for $\beta = 8$.

Table 4. The Comparison between BER Theory and BER SG under AWGN channel versus E_b/N_0 at β =16.

E_b/N_0 [dB]	σ	BER Theory	BER SG
0	*2.8147*	*0.4068*	*0.4388*
1	*2.5086*	*0.3849*	*0.3836*
2	*2.2358*	*0.3587*	*0.3516*
3	*1.9927*	*0.3277*	*0.3197*
4	*1.7760*	*0.2919*	*0.2863*
5	*1.582*	*0.2517*	*0.2372*
6	*1.4107*	*0.2080*	*0.1978*
7	*1.2573*	*0.1629*	*0.1599*
8	*1.1206*	*0.1191*	*0.1068*
9	*0.9987*	*0.0478*	*0.06*
10	*0.8901*	*0.0249*	*0.03995*
11	*0.7933*	*0.0109*	*0.04565*
12	*0.707*	*0.0038*	*0.01599*
13	*0.6301*	*0.001*	*0.01279*
14	0.5616	*0.0002*	*0*
15	0.5005	0	0
16	0.4461	0	0
17	0.3976	0	0
18	0.3543	0	0
19	0.3158	0	0
20	*0.2815*	0	0

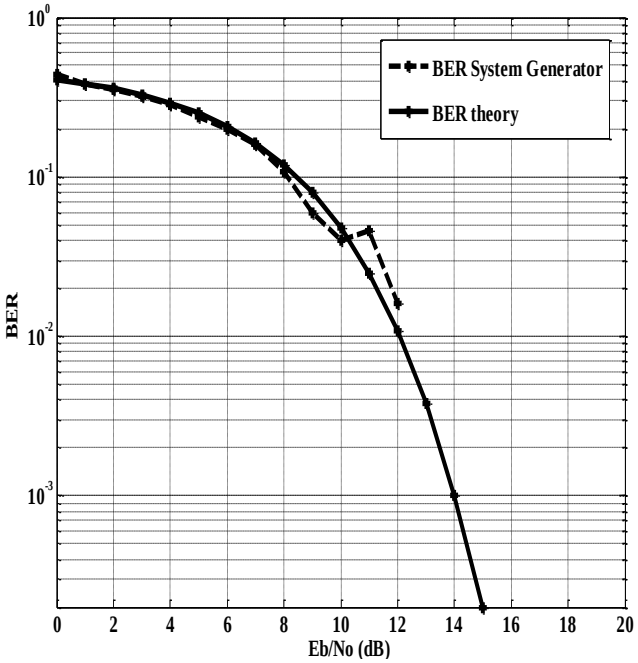


Figure 16. BER comparison of DCSK system between theory and SG results for $\beta = 16$.

Table 5. The Comparison between BER Theory and BER SG under AWGN channel versus E_b/N_0 at β =32.

E_b/N_0 [dB]	σ	BER Theory	BER SG
0	*3.9804*	*0.4319*	*0.4216*
1	*3.5475*	*0.4152*	*0.4216*
2	*3.1617*	*0.3946*	*0.3912*
3	*2.8179*	*0.3697*	*0.3574*
4	*2.5115*	*0.3399*	*0.3196*
5	*2.2383*	*0.3047*	*0.3196*
6	*1.9949*	*0.2644*	*0.2555*
7	*1.778*	*0.2197*	*0.2126*
8	*1.5846*	*0.1724*	*0.2126*
9	*1.4123*	*0.1255*	*0.1277*
10	*1.2587*	*0.0828*	*0.1277*
11	*1.1218*	*0.048*	*0.06394*
12	*0.9998*	*0.0235*	*0.03661*
13	*0.8911*	*0.0093*	*0.03661*
14	*0.7942*	*0.0028*	*0*
15	0.7078	0.0006	0
16	0.6309	0.0001	0
17	0.5622	0	0
18	0.5011	0	0
19	0.4466	0	0
20	0.3980	0	0

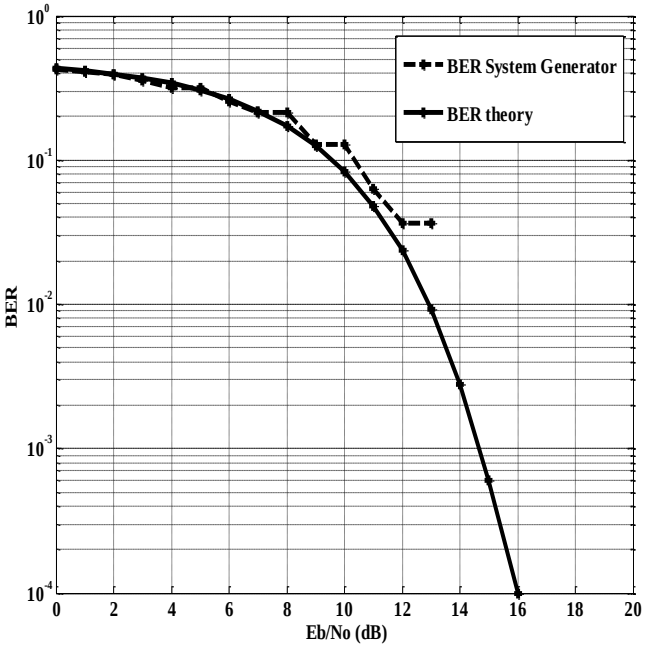


Figure 17.BER comparison of DCSK system between theory and SG results for $\beta = 32$.

5. FPGA Results

The DCSK system is performed by SP605 xc6slx45t-3fgg484 evaluation board with clock frequency 27 MHZ. ISE 14.5 is used with MATLAB R2011a. In this section, resource utilization report and hardware co-simulation results are presented.

5.1. Resource utilization summary

Table (6) and (7) illustrate the timing summary of DCSK modulation and demodulation respectively for different values of β. Table (8) and (9) illustrate the timing summary device utilization summary of DCSK modulation and demodulation respectively for different values of β.

Table 6. Timing summery of DCSK modulation for different values of β.

	β=4	***β=8***	***β=16***	***β=32***
Maximum Frequency (MHz)	34.252	40.016	39.287	39.587
Minimum Period (ns)	29.195	24.990	25.454	25.261
Peak Memory Usage (MB)	4619	4615	4615	4616

Table 7. Timing summery of DCSK demodulation for different values of β.

	β=4	***β=8***	***β=16***	***β=32***
Maximum Frequency (MHz)	74.705	65.291	51.733	41.592
Minimum Period (ns)	13.386	15.316	19.330	24.043
Peak Memory Usage (MB)	4625	4630	4630	4662

Table 7. Device utilization summary of DCSK modulation for different values of β.

		β=4		**β=8**		**β=16**		**β=32**	
Slice Logic Utilization	Available	Utilization	Used	Utilization	Used	Utilization	Used	Utilization	Used
Number of Slice Registers	54,576	1%	101	1%	66	1%	67	1%	88
Number of Slice LUTs	27,288	1%	92	1%	66	1%	67	1%	83
Number used as logic	27,288	1%	74	1%	51	1%	52	1%	53
Number used as Memory	6,408	1%	17	1%	12	1%	12	1%	24
Number of occupied Slices	6,822	1%	45		1		1		1
Number of MUXCYs used	13,644	1%	36	1%	38	1%	41	1%	39
Number of RAMB8BWERs	232	1%	1	1%	1	1%	1	1%	1
Number of BUFG/BUFGMUXs	16	6%	1	6%	1	6%	1	6%	1
Number of DSP48A1s	58	13%	8	13%	8	13%	8	13%	8
Average Fanout of Non-Clock Nets			1.34		1.43		1.43		1.42

Table 9. Device utilization summary of DCSK demodulation for different values of β.

		β=4		β=8		β=16		β=32	
Slice Logic Utilization	Available	Used	Utilization	Used	Utilization	Used	Utilization	Used	Utilization
Number of Slice Registers	54,576	944	1%	1,137	2%	1,031	1%	2,057	3%
Number of Slice LUTs	27,288	722	2%	885	3%	775	2%	1,480	5%
Number used as logic	27,288	413	1%	517	1%	515	1%	1,058	3%
Number used as Memory	6,408	248	3%	248	3%	4	1%	7	1%
Number of occupied Slices	6,822	302	4%	388	5%	332	4%	640	9%
Number of MUXCYs used	13,644	128	1%	240	1%	548	4%	1,128	8%
Number of fully used LUT-FF pairs	913	456	49%	520	45%	306	24%	643	25%
Number of slice register sites lost to control set restrictions	54,576	1	1%	8	1%	5	1%	8	1%
Number of RAMB8BWERs	232	8	3%	8	3%	0	0%	0	0%
Number of BUFG/BUFGMUXs	16	1	6%	1	6%	1	6%	1	6%
Number of DSP48A1s	58	8	13%	12	20%	16	27%	32	55%
Average Fanout of Non-Clock Nets		1.84		1.93		2.01		1.99	

5.2. Hardware co-simulation Results

The hardware co-simulation of DCSK system is performed on SP605 xc6slx45t-3fgg484 evaluation board with clock frequency 27 MHZ. The data input loaded in to the FPGA kit via Joint Test Action Group (JTAG) port. After processing, the data output from FPGA kit send back to the PC to compare with system generator results. Figure (18) and (19) show the FPGA hardware co-simulation for DCSK modulation and DCSK demodulation respectively at $\beta = 32$. It can be seen that the results are identical and this meaning that the system model has been successfully loaded onto FPGA board.

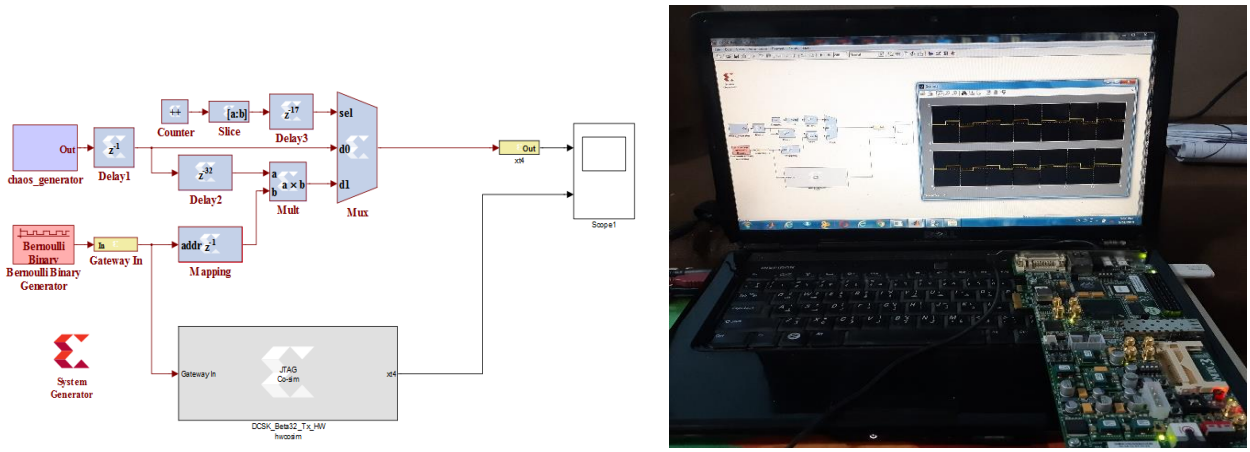


Figure 18. Hardware co-simulation of DCSK modulation at $\beta = 32$.

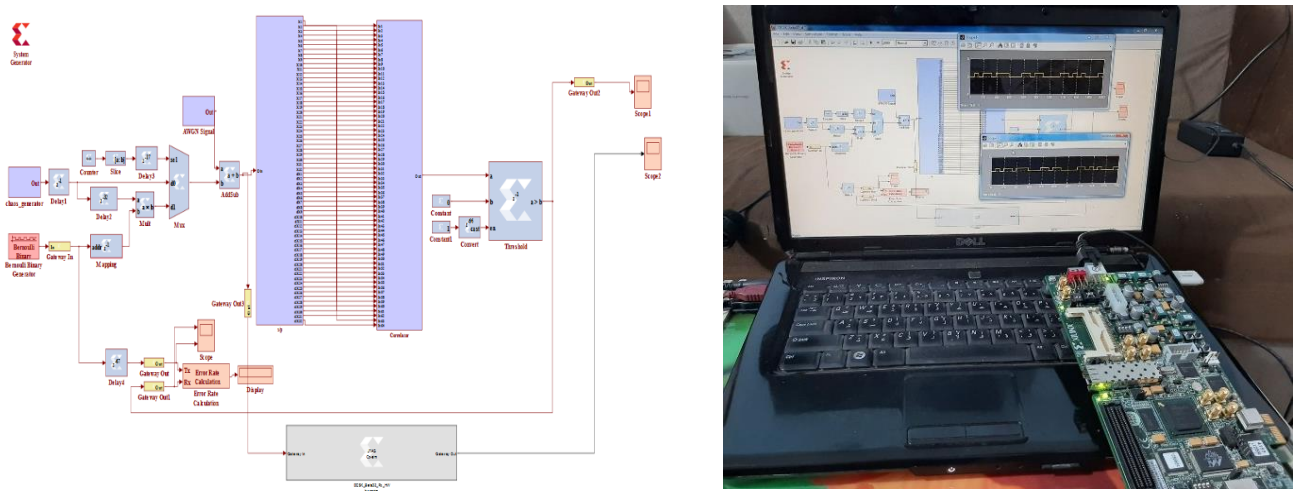


Figure 19. Hardware co-simulation of DCSK demodulation at $\beta = 32$.

6. Conclusion

In this paper, the design, and implementation of the DCSK system under AWGN channel is performed by the XSG software tools. DCSK is an analog circuit, therefore, we have been redesign to be suitable to FPGA. It is easier to be implemented the proposed system using XSG tools rather than VHDL code. The test 0-1 is used to test the chaotic signal if it is a regular or chaotic signal. The results show that the fixed point gives the best way to design the chaotic maps with low cost comparing with the floating point without any changing in the characteristics of the chaos system. The comparing between the BER analytical and system generator results for different spread factor, β, is studied. In general, when β increasing the BER performance of the

system increasing and complexity of the system is also increased. The hardware co-simulation of DCSK system is performed on SP605 xc6slx45t-3fgg484 evaluation board with clock frequency 27 MHZ. The results of hardware simulation prove that the system is worked in correct form.

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Conflict of interest

The authors have no conflicts of interest to declare.

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