LDPC Error Floor Improvement

Aseel Hameed Majeed
Electrical and Electronic College Techniques /Baghdad
Email:asu-hameed@yahoo.com

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ABSTRACT

The error-correcting performance of low-density parity check (LDPC) codes, when decoded using practical iterative decoding algorithms, is known to be close to Shannon limits. In this paper we study the LDPC codes performance when varying code rate, constellation level and the maximum number of iteration, this paper shows better coding gain can be obtained at the cost of higher complexity or higher bit rate. For some cases, due to their inability to reach very low bit error rates (e.g., 10^{-12}) at low signal-to-noise ratios (SNRs), a consequence the error rate floor phenomenon associated with iterative LDPC decoders is produced. This paper demonstrates that the concatenation system used LDPC as an inner code and the Bose, Chaudhuri, and Hocquenghem codes (BCH) as an outer code can successfully lower the floor. Connecting BCH codes lower the LDPC BER floor by a factor(from 32 to 22) at about SNR (from -1dB to 1.8 dB) with the same overall cod rate(i.e without any reduction in the bandwith efficiency) and restricted few number of iteration (only 5 iterations).

Keywords: LDPC, BCH, Error Floor.

تحسين أرضية الخطأ لشفرة التفقد المتكافئ المنخفض الكثافة

الخلاصة

أن أداء شفرة التفقد المتكافئ المنخفض الكثافة (LDPC) في تصحيح الأخطاء عند فك الشفرة بأستخدام خوارزمية فك الشفرة التكرارية, يكون قريبا من الحدود التي وضعها العالم شانون. يتضمن هذا العمل دراسة اداء شفراتLDPC عند تغيير نسبة الشفرة, مستوى التكوكب والحد الأعلى لعدد التكرار, هذا المقال يظهر امكانية الحصول على ربح تشفير اعلى على حساب زيادة التعقيد او زيادة نسبة الأرسال. في بعض الحالات لاتسطيع شفرات LDPC الوصول الى نسبة خطأ قليلة (مثلا 10^{-12}) في قيم قليلة لنسب الأشارة الى الضوضاء(SNRs), نتيجة لهذا تنشأ ظاهرة ارضية نسبة الخطأ المتزامنة مع فك شفرات LDPC المتكررة. هذا المقال يظهر بوضوح ان النظام المتتابع المكون من LDPC كشفرة داخلية وشفرة the Bose, Chaudhuri, and Hocquenghem codes المعروفة بشفرة (BCH) كشفرة خارجية, هذا النظام قادر بنجاح على تقليل ارضية الخطأ. أن ربط (BCH) قلل ارضية الخطأ في شفرة LDPC بمقدار من 32 الى 22 عند حدود SNR من -1dB الى 1.8 dB مع نسبة شفرة متماثلة (عدم فقدان كفاءة النطاق) وتقصير عدد التكرار الى عدد قليل (5 تكرارات فقط).

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INTRODUCTION

This become widely recognized that a full utilization of the available bandwidth cannot be achieved without powerful error-control schemes[1]. LDPC codes are type of interest channel coding techniques in obtaining rates close to the Shannon channel capacity, besides LDPC codes have an easily parallelizable decoding algorithm which consists of simple operations such as addition, comparison and table look-up. Moreover the degree of parallelism is "adjustable" which makes it easy to trade-off throughput and complexity[2]. LDPC codes were discovered by Gallager in 1962, but they were not given much attention for decades as the technology at the time was not mature for efficient implementation[2]. In 1981, Tanner introduced a bipartite graphical representation of low-density parity-check matrices known as the Tanner graph. The use of Tanner graphs as a graphical interpretation of LDPC codes lead researchers to consider the use of existing iterative message-passing algorithms to decode LDPC codes, thus resulting in the rediscovery of LDPC codes[3].

At present, LDPC codes are included in several existing standards, such as:

1- Digital Video Broadcasting - Second Generation (DVB-S2) standard (2005) replaces the concatenated Reed-Solomon/convolutional coding approach of DVB-S with a concatenation of an outer BCH code and inner low density parity check (LDPC) code. Because of the possible LDPC code mis-correction (i.e., the LDPC decoding converges to a valid but wrong codeword), the outer BCH code used to to improve the overall error-correcting performance [4]. The result is a 30% increase in channel capacity over DVB-S.[5]

2- IEEE 802.11n (2009) standard for wireless local area networks (WLANs)[6].

3- G.hn/G.9960 (2009), Telecommunication Standardization Sector (ITU-T), International Telecommunication Union (ITU), standard for networking over power lines, phone lines and coaxial cable[6].

4- IEEE Std 802.16e- (2006) standard, also called Mobile Wireless MAN or Worldwide Interoperability for Microwave Access (WiMAX)[6].

5- IEEE Std 802.3an (2006) standard for 10GBase-T Ethernet[6].

Despite of the powerful capability of the LDPC codes, simulation of LDPC codes performed on high speed hardware platforms indicate that LDPC codes, even regular ones do exhibit error floors[7]. The error probability performance curve of codes usually exhibits a steep transition region, the so-called waterfall (WF) region, followed by a more gently sloping plateau region referred to as the error floor (EF) region. In the error floor region virtually all failures are due to near Codewords, they are a consequence of frequently occurring error blocks, with a small number of systematic bit errors in each error block [7].

Many coding applications among them satellite communications, Ethernet transmission, and data storage applications require very low error rates, so that an important problem is the development of practical tools to clean up these residual errors and lower the floor [8]. A few researches have been devoted to the floor-lowering techniques at the decoder [9]. Others modifying the code itself [10], but the design of low-floor LDPC code systems is very difficult because they are not amenable to analysis, and simulations down to the 10^{-10} bit error rate (BER) region required a lot of time on even the fastest computers. [11]

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The most natural solution is by adding a properly designed outer algebraic code. To improve overall system performances, BCH codes can be used as an outer code in conjunction serially with LDPC Because of its powerful error-correcting capability and efficient decoding scheme, binary BCH codes are one of the most important linear block codes. Recently, with the intense interests on LDPC codes, a concatenation coding scheme with LDPC codes as inner codes while binary BCH codes as outer codes is widely accepted and finds its applications. [12]

Concatenated codes are efficient in wireless communication channels for two reasons. The first reason is that they have comparatively high minimum distances. On the other hand, the concatenated codes have the proper structure for burst error correction without the need for extra interleaving.[13]

In this paper the concept of concatenation system was adopt to study the ability of BCH codes to lowering the floor of the LDPC while keeping the same code rate. The rest of this paper is organized as follows: In section II and III the structure of LDPC code and BCH code are presented respectively. System model is explained in section IV. The simulation results are illustrated in section V and finally the conclusion derived from the results are presented in section VI.

LDPC CODES

LDPC codes can be described by a sparse parity-check matrix H containing a sparse number of non-zero entries. The term low-density means that the number of ones in each column and row of the parity-check matrix is small compared to the block size. Linear codes are defined in terms of generator and parity-check matrices. Generator matrix G maps information u to transmitted blocks x called codewords. For a generator matrix G, there is a parity-check matrix H which is related as $G \cdot H^{T} = 0$. All codewords must satisfy $x \cdot H^{T} = 0$ in terms of the parity-check matrix H. If the parity-check matrix H has the same weight per row and the same weight per column, the resulting LDPC codes is called regular. We use a two tuple (dv, dc) to represent a regular LDPC code whose column weight is dv and row weight is dc. When the weight in every column is not the same in the parity- check matrix, the code is known as an irregular LDPC code[14].

LDPC representation

Generally there are two different methods to represent LDPC codes. Like all linear block codes they can be described via matrices. The second method is a graphical representation[15].

Matrix representation

The matrix defined in equation (1) is a parity check matrix with dimension $n \times m$ for a (8, 4) code. We can now define two numbers describing these matrixes. wr

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for the number of 1's in each row and wc for the columns. For a matrix to be called low-density the two conditions *wc* << *n* and *wr* << *m* must be satisfied[15].

$$\mathbf{H} = \begin{bmatrix} 0 & 1 & 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 1 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 & 1 & 0 \end{bmatrix} \quad \ldots\ldots (1)$$

Tanner graph representation

The two types of nodes in a Tanner graph are called variable nodes (v-nodes) and check nodes (c-nodes). Fig. (1) is an example for such a Tanner graph and represents the same code as the matrix in (1). The creation of such a graph is rather straight forward. It consists of *m* check nodes (the number of parity bits) and n variable nodes (the number of bits in a codeword). Check node *fi* is connected to variable node *cj* if the element *hij* of H is a 1. [15]

Encoding Algorithm

Two encoding schemes are presented. The first encoding scheme is to deal with the generator matrix, and the second encoding scheme is to deal with lower triangular shape parity-check matrix[14].

Encoding Algorithm with Generator Matrix

Consider a linear block code with a generator matrix *G*. This encoding algorithm can be expressed by

$$x = u \cdot G \qquad \ldots. (2)$$

where the matrix *G* is of dimension $k \times n$, *u* is the information bits of dimension $1 \times k$, and *x* is the resulting codeword of dimension $1 \times n$. Using Gaussian-Jordan elimination and column ordering, it is always possible to obtain a generator matrix with following form

$$H_{(n-k)\times n} = [P_{(n-k)\times k}\, I_{(n-k)\times(n-k)}] \quad \ldots..(3)$$

$$G_{k\times n} = [I_k\, P^T_{k\times(n-k)}] \qquad \ldots.. (4)$$

where the matrix *I* is an identity matrix and the matrix *P* is a binary matrix. The generator matrix of LDPC codes is usually not sparse because of inversion. Cleary, when a data block *u* is encoded using a systematic generator matrix *G* in equation (3) and (4) , it is embedded without any modification in the last *k* coordinates of the resulting codeword. This encoding process requires $k\times (n - k)$ operations and has a computational complexity that is quadratic in the block length. Thus, this method is not suited for encoding LDPC codes with long block lengths.

Encoding Algorithm with Lower-Triangular Shape Parity-Check Matrix

To lower the complexity of the encoding process in the previous section, a Parity check matrix with an almost lower-triangular shape is created as depicted in

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Fig. (2). The idea in this method is to minimize the constant factor g in front of the quadratic dependency. Instead of computing the product $x = u \times G$, the equation $H \times x^T = 0$ is solved.

II-2 Decoding

This paper focuses on the sum-product decoding algorithm, and binary-phase-shift – keyed (BPSK) signaling (under the mapping $0 \rightarrow 1$ and $1 \rightarrow -1$). As with other iterative algorithms, the sum-product algorithm relies on the exchange of messages between bit nodes and check nodes to achieve correct bit decisions. Suppose the Tanner graph consists of n bit nodes and m check nodes. In the first step, bit nodes xi, $i = 1, 2,$-------, n, are initialized with the prior log likelihood ratios given in (5) below using the channel outputs yi, $i = 1, 2,$---------, n [8]

$$l_i = log\frac{p(x_i=0|y_i)}{p(x_i=1|y_i)} = \frac{2y_i}{\sigma^2} \qquad \text{.....(5)}$$

where σ denotes the standard deviation of noise in this Gaussian channel. Bit nodes first send the prior LLR messages to the neighboring check nodes along the edges of the Tanner graph, and the subsequent message exchange is governed by the bit-to-check message $Qi \rightarrow j$ and the check-to-bit message $Rj \rightarrow i$ as represented in (6) and (7)below respectively, where $N(i)$ refers to the neighborhood of the node i,

$$Q_{i\rightarrow j} = l_i + \sum_{k\epsilon N(i)\backslash j} R_{k\rightarrow i} \qquad \text{.....(6)}$$

$$R_{j\rightarrow i} = \prod_{l\epsilon N(j)\backslash i} sgn\left(Q_{l\rightarrow j}\right)\Phi^{-1}\left(\sum_{l\epsilon N(j)\backslash i}\Phi(|Q_{i\rightarrow j}|)\right) \qquad \text{.....(7)}$$

where $\Phi(x) := -\log[\tanh(x/2)]$ for $x \geq 0$. The posterior log-likelihood ratio at each bit node is then computed as:

$$LLR_i^{post} = l_i + \sum_{j\epsilon N(i)} R_{j\rightarrow i} \qquad \text{..... (8)}$$

The message passing algorithm is typically allowed to run for a fixed number of iterations, both because convergence is not guaranteed when many cycles are present, and due to practical (delay) constraints. Based on the posterior LLR, a bit-wise hard decision is made: " 0" if $LLR_i^{post} \geq 0$ and "1" otherwise.

BCH codes

An (N, K, t) BCH code has a block length of N bits and information length of K bits. While Operating under $GF(2^m)$, it has the error-correcting capability t, where $N\text{-}K \leq m \times t$. As shown in Fig. (3), the conventional BCH decoding contains three major steps. The received polynomial $R(x)$ is loaded into the First In First Out (FIFO) and fed into the syndrome calculator to generate syndrome polynomial [16].

$$S(x) = S_1 + S_2x^1 + \text{--------} + S_{2t}\,x^{2t-1} \qquad \text{.....(9)}$$

which is expressed as :

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$$S_j = R(\alpha^j) = \sum_{i=1}^{v} (\alpha^j)^{ei} = \sum_{i=1}^{v} (\beta_{ei})^j \quad for\ j = 1\sim 2 \quad \ldots.(10)$$

where α is the primitive element over *GF(2m)* and *v* is the number of actual errors. Notice that *ei* is the ith actual error location and β_{ei} indicates the corresponding error locator. The key equation solver is used to carry out the error location polynomial *σ(x)*, which is defined as:[16]

$$\sigma(x)=(1+x\beta_{e1})(1+x\beta_{e2}).....(1+\beta_{ev})$$

$$= 1 + \sigma_1 x^1 + \sigma_2 x^2 \ldots + \sigma_v x^v \quad \ldots. (11)$$

The key equation describing the relation between *S(x)* and *σ(x)* is derived as:

$$\Omega(x) = S(x) \times \sigma(x)\ mod\ x^{2t} \quad \ldots\ldots(12)$$

where *Ω(x)* is the error evaluator polynomial. The most popular methods for solving the key equation are Berlekamp–Massey and modified Euclidean algorithms . After the key equation solver, Chien search is applied to find the roots of σ(x). If an error is occurred at the e_ith position, α^{-ei} will be a root of *σ(x)*. Finally, the estimated codeword $\hat{C}(x)$polynomial is obtained by outputting *R(x)* from the FIFO and inversing those values at error locations[16].

System Model

The system model used is shown in Fig. (4), where the LDPC code used as the inner Code and BCH as the outer code. A message (x) for an [n,k] BCH code must be a k-column binary Galois array. The code (y) that corresponds to that message is an n-column binary Galois array. Each row of these Galois arrays represents one word. The codeword generated by the BCH encoder is then recoded by using LDPC encoder to produce a new codeword (z). After the coded bit sequence has been obtained, it is applied to different level of Phase Shift Key (M-PSK) modulator. This modulated waveform(c) is transmitted over AWGN channel, where the noise is assumed to be additive white Gaussian noise with zero mean and variance σ^2. Finally The errors in the received signal ($\hat{c}$) are detected and corrected when passing through the demodulator and the decoders.

Simulation And Results

The simulation results is divided into two sections the first one dealing with the evaluation of Low Density Parity Check code(LDPC) performance when varying the parameters related to its frame work. The second section focus on improving the LDPC performance by concatenated it with Bose, Chaudhuri, and Hocquenghem codes (BCH code). Both sections were implemented using Matlab 2011a.

LDPC evaluation

Investigate the relation between the number of iteration and other parameters

The LDPC performance was studied for each codeword in a set of 20 codewords to count the number of decoder iteration until the parity checks are all satisfied, while varying code rate, constellation level and SNR. The results are illustrated in Fig. (5),(6) and (7) respectively.

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The results obviously show that reducing the code rate or reducing the constellation level lead to reducing the number of iteration, While the SNR reduction has the opposite effect. This results are documented in table (1).

Investigate the relation between the number of iteration and BER

The average BER was calculated for the 20 codewords when the LDPC number of iteration was restricted to a finite number. The simulation results represented by Fig. (8), (9), and (10) are abstracted in table (2) . These results show clearly two ideas:

A. By little increasing in SNR, the number of iteration can be reduced, which means speed up the simulation and achieving the same BER. For example for QPSK modulated signal, increasing SNR from 1dB to 2dB, the number of iteration can be reduced by 15 while achieving the same BER of 10^{-4}.

B. For each modulation level, there is a certain value of SNR which considered being the effective value where good performance can be obtained. This is certainly due to the increasing of the bit rate to be transmitted which is demand more power. For example, BER below 10^{-1} cannot be achieved for an 16PSK modulated signal with SNR 7 dB even with the increasing the number of iteration. By trial and error the effective SNR values were found for each modulation level when the maximum number of iteration was limited to 50 as shown in table (2).

Investigate the relation between BER and SNR for different LDPC code rates

The performance of LDPC was evaluated in the form of BER against SNR with different code rates when 100 codeword are mapped to BPSK modulation and the decoder iteration was limited to 5, as shown in Fig. (11). The simulation results show that, there is a tradeoff between the throughput and the good performance.

Evaluation of system model:

Evaluation of LDPC with BPSK modulated signal

As mentioned before LDPC suffer from the error floor and in order to overcome this problem, BCH code is connected in series as an outer code. The performance of the concatenation system represented in figure(3) was evaluated, when the average of BER for 100 codeword mapped to BPSK modulation was calculated as shown in Fig. (12). It is clearly noticed the effectiveness of using BCH codes as outer codes. Its higher minimum distance results in improving the performance in the error floor region, while preserving a very good convergence behavior.

Fig.(13) explain a comparison between the performance of the LDPC with a code rate R_{LDPC} (section V-1-3) and the performance of the concatenation system with the same overall code $R_{BCH} \times R_{LDPC}$. For example, the LDPC performance with code rate 1/3 was compared with the concatenation system performance with BCH code rate 2/3 and LDPC code rate 1/2 to get an overall rate 1/3. As a result 1.6 dB code gain is obtained at BER of 10^{-7}.

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Evaluation of LDPC with different M-PSK modulated signal

The same comparison was done for different level of constellation QPSK, 8PSK and 16PSK with system over all code rate 1/3 as shown in Fig. (14). All the results confirm the gain value(˜ 1.4 dB at BER of 10^{-7}) obtained in the previous section.

CONCLUSIONS

Forward error correction scheme based on LDPC codes was evaluated . Set of different LDPC code rates with different modulation schemes was analyzed. Performance simulation for varying modulation level for such codes has been presented when changing the maximum number of iterations and the results show that the same BER can be obtained while reducing number of iterations at the cost of little SNR increasing, which is a good approach for decoding huge data when real time concept is considered.

Varying code rate shows generally the lower the code rate, the higher the coding gains, with code rate 1/4 BER of 10^{-7} can be achieved at the cost of 0.2 dB only.

Despite of many LDPC unique features, the error floor phenomenon associated with iterative LDPC decoder is produced as a consequence due to their inability to reach very low bit error rates at low SNRs especially with higher code rate. We conclude that connected BCH codes serially with LDPC can successfully lower the error floor by a factor(from 32 to 22) at about SNR (from -1dB to 1.8 dB) while supporting the same code rates for a BPSK modulated signal. Certainly low BER (e.g. 10^{-12}) can be achieved ,but this demands huge computational tasks which of course required running the program for days. In other word, better Codes provides better coding gains and higher complexity. The basic idea is that, for each LDPC code decoding failure, we use the hard decisions of the inner LDPC decoding iterations as the input to the successive BCH code decoder until the BCH code decoder succeeds.

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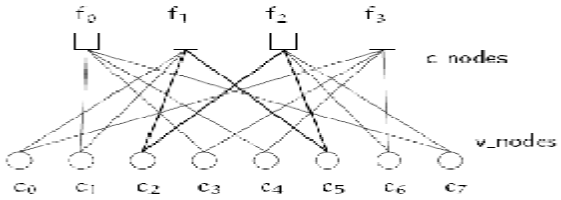
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Table (1) Average number of iteration vrs. Code rate, constellation level and SNR

System parameters		Average number of iteration for 20 frame
SNR = 1 QPSK Modulation	Code rate = 1/4	10
	Code rate = 1/2	30
SNR = 8 Code rate =1/2	QPSK	2
	8PSK	5
	16PSK	21
QPSK Modulation Code rate =1/2	SNR= 1	31
	SNR =2	13

Table(2) SNR vrs. Number of iteration and modulation level

Modulation	Effective SNR	SNR required to achieve BER of 10^{-4}	
		Number of iteration reduced to 20	Number of iteration reduced to 10
QPSK	1 dB	1.2 dB	2 Db
8PSK	4 dB	4.4 dB	5.2 dB
16PSK	7.5 dB	8 dB	9 dB



Figure(1) Tanner graph corresponding to the parity check matrix in equation (1)

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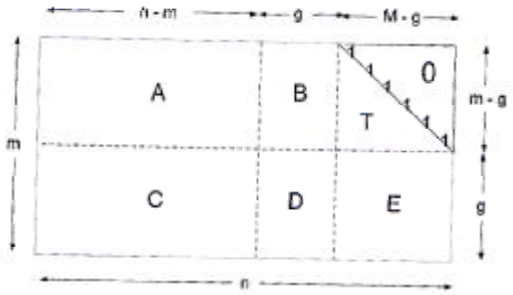


Figure (2) Parity-check matrix in approximate lower triangular form.

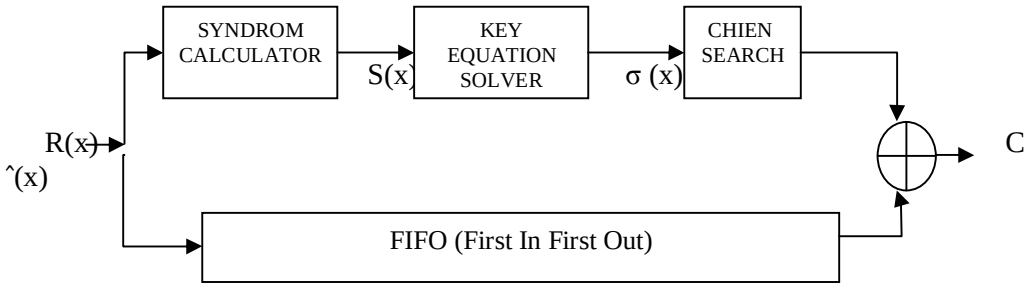


Figure (3) Binary BCH decoding process

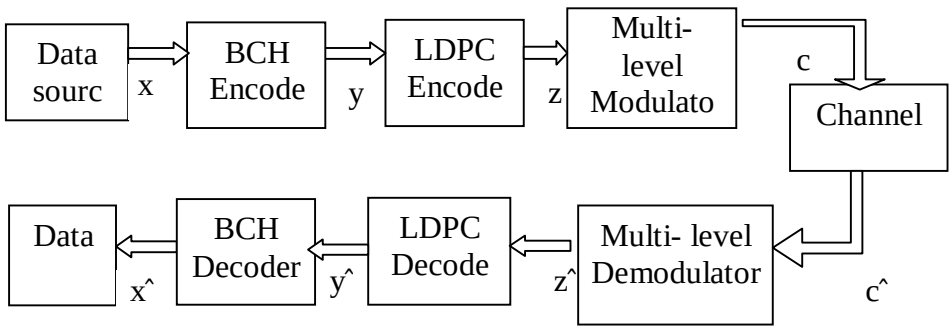


Figure (4) System Model

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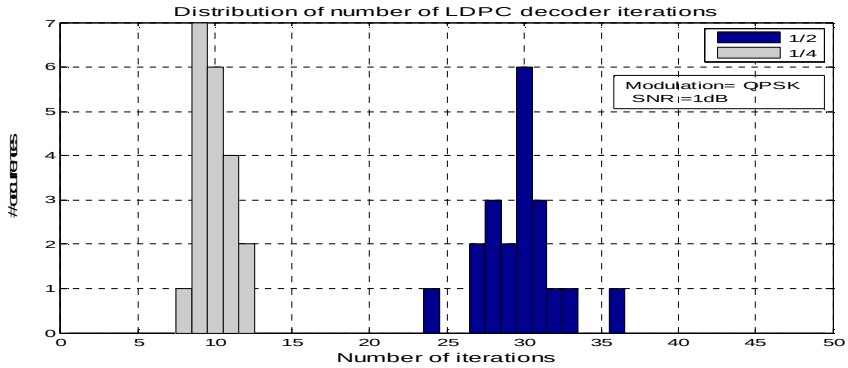


Figure (5) Distribution of number of LDPC decoder iterations for different code rate

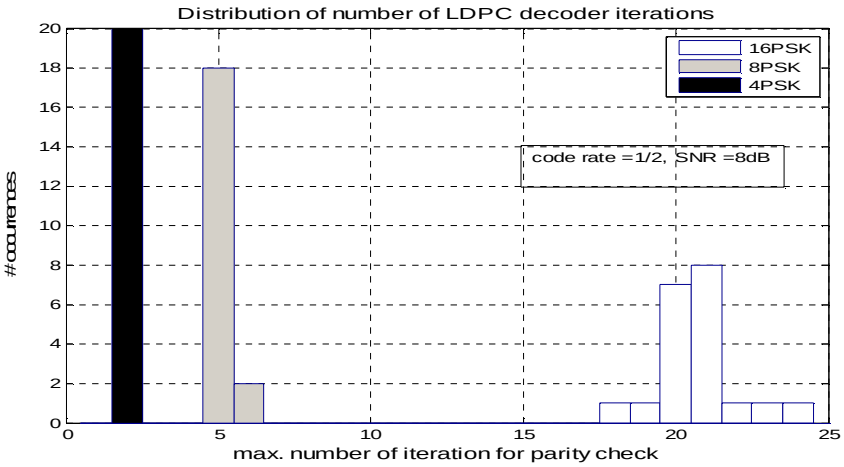


Figure (6) Distribution of number of LDPC decoder iterations for different level of constellation

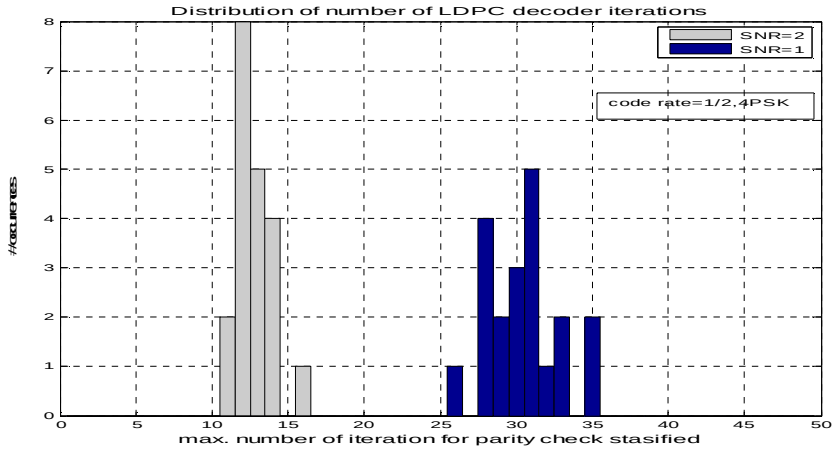


Figure (7) Distribution of number of LDPC decoder iterations for different value of SNR

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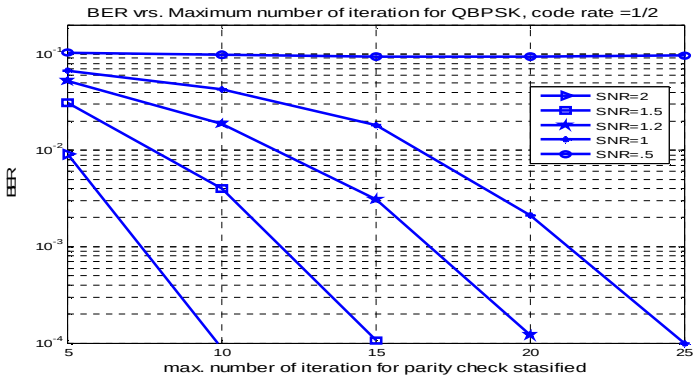


Figure (8) BER vrs. LDPC decoder iteration for different values of SNR, code rate=1/2, constellation(4PSK)

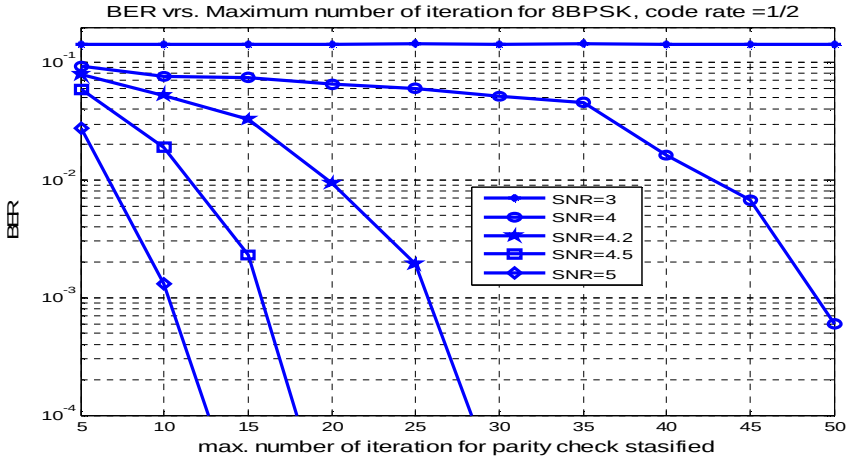


Figure (9) BER vrs. LDPC decoder iteration for different values of SNR, code rate=1/2, constellation= 8PSK

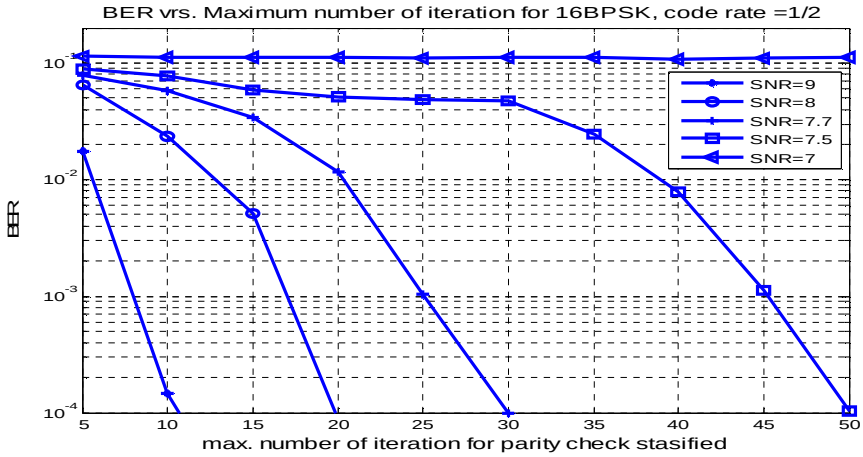


Figure (10) BER vrs. LDPC decoder iteration for different values of SNR, code rate=1/2, constellation= 16PSK

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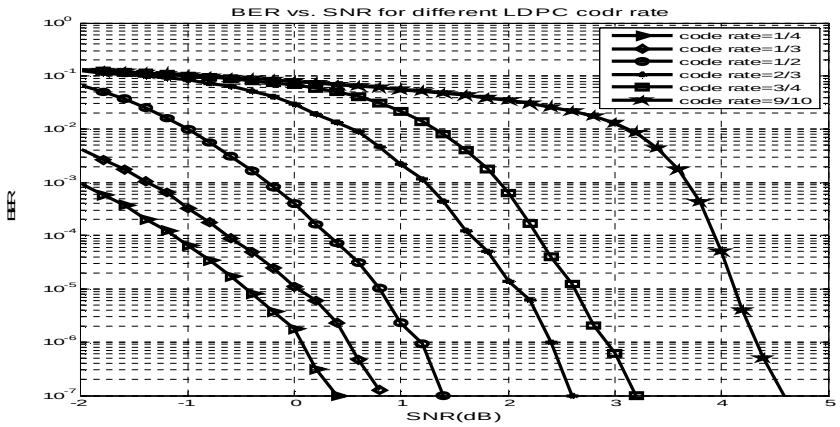


Figure (11) BER vs. SNR for different LDPC code rate, constellation(BPSK)

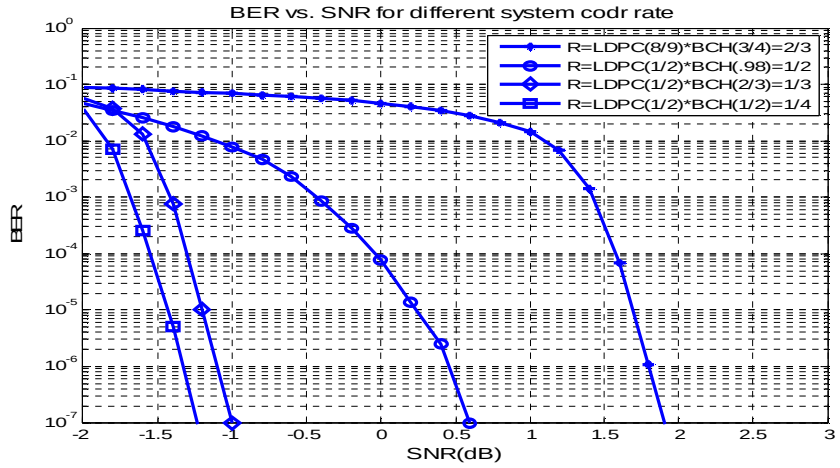


Figure (12) BER vs. SNR for different over all code rate, constellation= BPSK,

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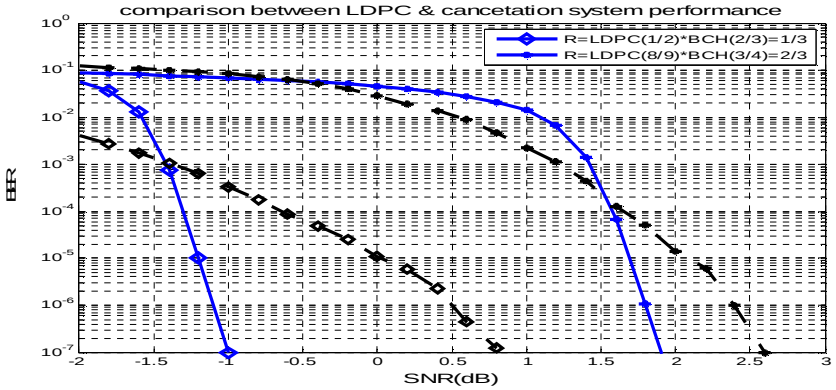


Figure (13) Comparing between LDPC performance and (BCH&LDPC) performance, constellation= BPSK

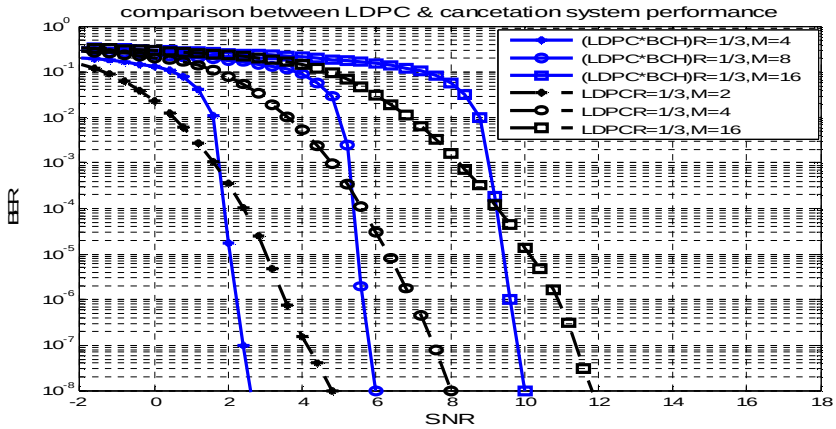


Figure (14)Comparing between LDPC performance and (BCH&LDPC) performance for different level of constellation

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