Fabrication and characterization of feasible heterojunction bipolar transistor (HBT) made by depositing of p-type CdS film on monocrystalline silicon homojunction were demonstrated. The ideality factors (n) of emitter-base and base-collector abrupt junctions were 1.6 and 1.8 respectively. The transistor exhibited current gain $\beta_{dc}$ as high as 360.

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1. Introduction
Possibility of using wide-bandgap emitter injection efficiency of a transistor was first proposed by Schockley [1] and later analyzed by Kroemer [2] in 1957. Even though this idea promised large advantages over the existing transistors, very little attention was paid towards the realization of such a transistor due to rapid advances in the technology of homo-transistor [3, 4]. With the advancement in the "state of art" of heterojunction fabrication [5-7], the interest in the heterojunction bipolar transistors (HBTs) has been lately revived [8-11]. The recent trend in high-speed silicon technologies has produced remarkable advances in silicon-based HBT. The physical structure of such a transistor is composed of a hetero-layer (emitter) grows on a p-n Si diode. The grown layer can be formed by several techniques. Among the various techniques, spray pyrolysis was used successfully in producing heterojunction [12,13]. In this paper, a newly found junction characteristics of the (p)CdS-(n)Si-(p)Si HBT are presented where p-CdS was grown by spray pyrolysis.

2. Experiment
Boron-doped single crystal p-Si wafer with sheet resistivity of about 35.6 $\Omega$/sq. and orientation of (100) has been thermally diffused by phosphorus using thermal diffusion system. The diffused layer was heavily doped (2.1x10^{18}cm^{-3}) and the junction was made to be 0.5µm. Wide-emitter p-CdS:Ag layer with thickness of 1µm and area of 0.7mm$^2$ has been deposited onto n-Si side by pyrolytic spraying of an aqueous solution of 0.2M CdCl$_2$, 0.18M thiourea and 0.006M AgNO$_3$ with a deposition rate of about 2nm/s. The preparation substrate temperature was 350°C. Figure 1 depicts a photograph of spray pyrolysis apparatus used in this study. Indium, gold and aluminium electrodes were deposited by thermal evaporation through special masks on CdS:Ag, n-Si and p-Si respectively. Figure (2) displays energy band diagram of fabricated HBT. Hall measurements were done to estimate the conductivity type of CdS:Ag layer deposited on glass substrate. C-V measurement of HBT at 1MHz was carried out using LCZ system.

3. Results and Discussion
Pure CdS is normally an n-type semiconductor. This type of conductivity is essentially due to the non-stoichiometry arisen from the excess Cd in the CdS lattice (enriched-Cd). So that it is previously used as a heterojunction transistor type n-p-n with n-pSi diode [14] and/or window layer for UV-enhancement in double junctions with p-nSi photodiodes [15]. Producing p-type CdS can be obtained by silver doping of CdS. In this doping, Cd$^{2+}$ will be replaced by Ag$^+$ in the lattice of CdS microcrystallites. This replacement will result in less sulfur deficiency because the anion (S$^{2-}$) has a valence number greater than the cation (Ag$^{+}$) and

Fig. (1): Spray pyrolysis system used to grow CdS:Ag layer
enriched-S CdS will be produced. This type of defects leads to abundant of holes and p-type CdS will be formed. Hall measurement of Ag-doped CdS shown in Figure 3. This figure shows a p-type behavior, so that it will form a heterojunction transistor type p-n-p with p-nSi.

Fig. (2): An equilibrium band diagram of (p)CdS-(n)Si-(p)Si HBT

Fig. (3): The relationship between Hall voltage and passing current for p-CdS film

The two junctions of the triode have been characterized separately using I-V measurements. Figure 4a demonstrates $I_E-V_{EB}$ characteristics (floating collector) where $V_{BE}$ and $I_E$ respectively represent the applied voltage across emitter-base junction and the flow current due to this voltage. The forward current of this junction is distinguished by two regions, the first (less than 0.3V bias voltage) region represents recombination mechanism while the second (greater than 0.3V bias voltage) indicates tunneling mechanism. The transport mechanism then shows good conformity with the tunneling-recombination model. This result is in full agreement with those of p-Cds/n-Si heterodiode [16]. Figure 4b illustrates the $I_C-V_{BC}$ characteristics (floating emitter) where $V_{BC}$ and $I_C$ respectively represent the applied voltage across base-collector junction and the flowing current due to this voltage. The $I_C-V_{BC}$ curve of this junction shows a behavior in coincidence with that of Shockley model ($I=I_0 \exp(qV/nkT)$). High leakage current reflects the heavily doped layer. From the two plots of Figure 4, the ideality factor ($n$) of emitter-base and base-collector junctions were as low as 1.6 and 1.8, respectively, indicating high quality of both junctions. Figure 5 presents $C_{EB}-V_{EB}$ and $C_{BC}-V_{BC}$ curves where the subscripts refer to the emitter-base and base-collector, respectively. It is shown from the figure that the emitter-base junction capacitance is smaller than that of base-collector. This can be elucidated by the low carrier concentration of the wide-emitter. On the other hand, these two junctions are abrupt types.

Fig. (4): I-V characteristics for (a): (p)CdS-(n)Si junction and (b): (n)Si-(p)Si junction

The dc beta ($\beta_{dc}$) of the common-emitter HBT has been directly measured and gave a value of 360, this high value has been obtained using material for which there is a large lattice mismatch of roughly 8% and indicates that interfacial recombination is much less than has been generally anticipated, this is
mainly due to forming the gate layer (the base) with its high electron density in defect-free single-crystal material. The experimental HBT constructed in the present work is not optimized in any way, but serves merely to demonstrate the feasibility of transistor action. Considerable further research remains to be done to optimize the transistor performance and to ascertain the best design parameters.

4. Conclusions
A high dc performance heterojunction bipolar transistor has been realized by the low-cost spray pyrolysis technique. This technique allows good price/quality ratio. The relatively high value of dc beta (360) demonstrates clearly that the HBT type (p)CdS-(n)Si-(p)Si is a practical proposition.

References

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