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Design Band Energy diagram of SnO_2/CdS-CdTe Thin Film Heterojunction Using *I-V* an d *C-V* Measurements

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ABSTRACT

SnO_2/CdS-CdTe heterojunction has been fabricated by thermal evaporation technique, 0.05 µm thicknesses of SnO_2 nanostructure was evaporated as thin layer to be used as an antireflection and as transparent conducting oxide. The prepared cell has been annealed at 573K for 180 minutes. The general morphology of SnO_2 films was imaged by using Atomic Force Microscope (AFM), the image shows that the average grain size of the prepared film is constructed from nanostructure of dimensions in order of 72 nm. There are two wide peaks were presents at the x-ray pattern which were refers to SnO_2 and is in agreement with the literature of American Standard of Testing Materials (ASTM).

The capacitance- voltage a measurement has studied at 10^2 Hz frequency, the capacitance- voltage measurements indicated that these cells are abrupt. The capacitance at zero bias, built in voltage, zero bias depletion region width and the carrier concentration have been calculated. The carrier transport mechanism for SnO_2/CdS-CdTe heterojunction in dark is tunneling – recombination. The value of ideality factor is 1.56 and the reverse saturation current is 9.6×10^{-10}A. Band energy lineup for SnO_2/ n-CdS-p-CdTe heterojunction has been investigated by using *I-V* and *C-V* measurements.

Key words: n-CdS-p-CdTe Heterojunction; C-V Measurements; I-V Measurements; Energy Band Diagram.

رسم مخطط الطاقة للمفرق الهجين للغشاء SnO_2/CdS-CdTe الرقيق باستخدام قياسات تيار – جهد و سعة – جهد

الخلاصة

تم تحضير المفرق الهجيني SnO_2/CdS-CdTe بتقنية التبخير الفراغي الحراري,واستعمل غشاء من SnO_2 ذو التركيب الناوي المحضر بسمك 0.05 µm كطبقة شفافة ضد الانعكاسية , ثم تم تلدين المفرق المحضر بدرجة 573 مئوية ولمدة 180 دقيقة. تم فحص تركيب غشاء SnO_2 باستخدام المجهر الالكتروني(AFM) , وقد تبين بان الغشاء ذو تركيب نانوي بمعدل للحجم البلوري

72 نانومتر, ومن تحليل لنتائج فحوصات حيود الاشعة السينية تبين بالشكل عن وجود قمتين واسعة تشير للمادة المحضرة طبقا للمقاييس الامريكية لفحوصات المواد (ASTM) .

تم دراسة قياسات سعة – جهد عند تردد 100 هرتز, و قد اشارت هذه القياسات الى ان تلك المفارق هي من النوع الحاد. و قد وجد ان قيمة السعة عند الانحياز الصفري و جهد البناء الداخلي قد تناقصا بعد عملية التلدين. بينما يزداد عرض منطقة النظوب للانحياز الصفري و تركيز الحاملات مع عملية التلدين. و كانت ميكانيكية انتقال الحاملات للمفرق الهجيني عند الظلام هي أنتفاق-اعادة اتحاد. و كانت قيمة عامل المثالية 1.56 و تيار الاشباع هي 9.6×10^{-10}أمبير. و تم ايضا دراسة مخطط حزمة الطاقة عن طريق قياسات تيار – جهد و سعة – جهد.

INTRODUCTION

CdS/CdT thin-film photovoltaic (PV) technology plays a key role in today's fast growing photovoltaic industry [1]. Details about processing conditions like maximum processing temperatures are not known [2]. By the use of low growth temperatures not only production cost and energy payback time can be reduced, but also thermally sensitive substrates like polyimide film can be used [2]. CdTe, in the form of a compound, is stable in air and has no toxicity to the environment [3]. The material cost is relatively low compared to other solar cells, such as the Si based crystalline solar cell, which is currently dominating the solar cell market [3]. CdTe has been recognized as an attractive photovoltaic material because of its direct band gap (E_g) around 1.5 eV, which is near the optimal value for p-n devices. The absorber thickness in commercial CdS/CdTe PVs is in the range of 5-10 μm [4]. CdTe thickness could be as small as 1 μm to absorb about 90% of incident solar light [4]. Cadmium sulfide (CdS) belonging to the II-VI group is one of the promising materials for optoelectronic devices [5]. Capacitance vs. voltage is one of the most important techniques for the device characterization. This technique, together with the current–voltage measurements permit to study the transport mechanism in the heterostructure and the basic physical parameters and junction features. The gained information is essential for understanding the photovoltaic loss mechanism, thus to improve the PV-device performance to get higher efficiencies [6]. In this article, it is reported a study of capacitance voltage characteristics and study the current voltage characteristics of thermally deposited CdS/CdTe heterojunctions, the band discontinuity and the interface charge density, which are obtained.

EXPERIMENTAL WORK

SnO_2/CdS-CdTe heterojunctions were produced via thermal evaporation technique. Corning glass used as a substrate, coated by Au of 0.05 μm thickness as back contact. p-CdTe layer with thickness of about 1.2 ± 0.05 μm evaporating on Au back contact layer, and then n-CdS layer with thickness of about 0.2 ± 0.05 μm evaporating on CdTe layer. Then nanostructure SnO_2 of 0.05 μm thicknesses was evaporated as thin layer to be used as an antireflection coating and as transparent conducting oxide, finally Al of 0.05 μm thicknesses as an electrode. The films have been deposited at substrate temperature 373 ± 5 K. All materials have 99.999% purity. The thicknesses of the prepared films were measured using Fizue method. The contacts of CdS on CdTe have been prepared in a sandwich configuration between Al and Au electrodes. The basic structure of the prepared heterojunction is shown in Figure (1). The Edward E306A coating system was used for all

deposition processes, under pressure of about 10^{-6} mbar, the prepared CdS/CdTe heterojunctions annealed at 573 ± 5 K 180 minutes under vacuum of 30 mbar. Keithley 616 digital electrometer has been used to measure the resistance of CdTe films. Capacitance-voltage (C-V) measurements under reverse bias voltage between zero to 1 volt with frequency of 10^2 Hz have been carried for CdS/CdTe heterojunction by HP-2RC unit model 4274A and 4275A multifrequency LCR meter. Current-voltage (I-V) measurements at the forward and reverse bias in dark, in addition to forward current measured at different ambient temperatures around room temperature of CdS/CdTe heterojunction were done by Keithley digital electrometer 616 and D.C. power supply.

RESULTS AND DISCUSSIONS

C-V Characteristics for SnO_2/CdS-CdTe heterojunction

Mott-Shcottky plot (C^{-2} vs. V) for SnO_2/CdS-CdTe heterojunction is shown in Figure (2), the plots reveal straight line relationships which mean that the junction was an abrupt type [7]. The capacitance (C) strongly depends on the applied bias and the slope of C^{-2} plot junction capacitance. In this case, it can be said that the Au/CdTe contact is well formed. Similar results have been found by Jun et al [8]. The depletion layer width (W) is defined as [7]:

$$W = \left(\frac{2e_1 e_2 (V_{bi} - V_a)(V_A - V_D)^2}{qN_D N_A (e_1 N_D - e_2 N_A)} \right)^{1/2} \quad \ldots (1)$$

Where ε_1 and ε_2 are the dielectric constants for n- and p-types semiconductor respectively, V_{bi} and V_a are the built-in and applied voltages respectively, q is the electron charge, N_D and N_A are the donor and acceptor concentration respectively. The doping concentration can be calculated from the following relation [7]:

$$C^{-2} = \left(\frac{2(e_1 V_A - e_2 V_D)^2}{qA^2 N_D N_A e_1 e_2} \right)^{1/2} (V_{bi} - V_a) \quad \ldots (2)$$

Where A is area of junction.

The intercept of the line that results from plotting between C^{-2} as a function of reverse bias represents the built-in potential and the carrier concentration can be calculated from the slope of this line from equation 3, the V_{bi} value is 0.92.The higher value of V_{bi} may be attributed to the midgap states that act as recombination centers that may arise either from states created as a result of junction fabrication or lattice mismatch between CdTe and CdS [9]. The capacitance measurement relies on the fact that the width (W) of the space-charge - region (SCR) of a semiconductor device junction changes with applied voltage. The value of depletion region width for SnO_2/CdS-CdTe cells is 0.43 μm. The acceptor concentration of SnO_2/CdS-CdTe heterojunction is 0.61×10^{16} (cm^{-3}). The values of doping concentration suggests that the SnO_2/CdS-CdTe interface is n^+p type, elsewhere, we have shown that in the case of n^+p type junction, recombination in the absorber space charge layer dominates over interface recombination [10].

The surface morphology of SnO_2

The general morphology of SnO_2 films was imaged by using Atomic Force Microscope (AFM), the image shows that the average grain size of the prepared film is constructed from nanostructure of dimensions in order of 72nm, as shown in Figure (3).

X-ray patterns of the nanostructure SnO_2

The X-ray diffraction of SnO_2 thin layer was obtained at two theta from 20˚ to 60˚ glancing angle; there are two wide peaks present at x-ray pattern, as shown in Figure (4). The result is in agreement with the literature of American Standard of Testing Materials (ASTM), as listed in Table (1), the highest peak observed at 2Θ equal 26.847°.

I-V Characteristics for SnO_2/CdS-CdTe heterojunction

Figure (5) shows the I-V Characteristic at dark of SnO_2/CdS-CdTe heterojunction. In general, the I-V characteristics for the SnO_2/CdS-CdTe heterojunction at forward bias voltage show that the forward current consists of two regions; the first region represents recombination currents while the second represents the tunneling currents [11]. The carrier transport mechanism for this case is of a tunneling–recombination type, in coherence with Alnajjar et al [9]. The reverse saturation current was calculated from the intercept of the straight line with the current axis at zero voltage bias. The value of reverse saturation current is 9.6×10^{-10}A. This result is in agreement with Alnajjar et al [9]. The ideality factor (β) can be calculated from the following relationship [7]:

$$b = \frac{q}{k_B T} \frac{V_F}{\ln\left(\frac{I_F}{I_S}\right)} \quad \ldots (3)$$

Where V_F is the forward bias voltage, I_F and I_S are the forward bias and the saturation currents respectively, β can be calculated by applying equation 4 to the first region of the upper curve. The value of ideality factor t is 1.58, similar result have found by Huijin et al [12].

Band energy diagram of SnO_2/CdS-CdTe solar cell

The values of energy gaps of CdS (E_{g1}) is near 2.4 eV [13] and of CdTe (E_{g2}) is 1.44 eV [14]. heterojunction has been investigated by using I-V and C-V measurements [15]. I-V measurements under forward bias in the temperatures range (291 -301) K. The measurements were taken at low voltages to cancel the role of the tunneling effect. We can observe that the I_S decreases with decreasing temperature due to resistance increase. Figure 6 shows the dependence of the I_S on the 10^3/T, from the slope of this figure the value of valence band offset (ΔE_v) can be deduced and by using the following equation [11]:

$$I_S = \exp\left(\frac{-q(V_D - \Delta E_V)}{k_B T}\right) \quad \ldots (4)$$

The value of ΔE_v which is calculated from the previous relation equals to 0.40 eV. The total built-in voltage (V_{bi}) is 0.92 eV, which is due to difference in work functions (ϕ) and it is equal to the sum of built-in voltages on both sides [11], therefore we can calculate the value of conduction band offset (ΔE_c) is 0.56 eV, which calculated from the following equation [16]:

$$\Delta E_C - \Delta E_V = E_{g1} - E_{g2} \quad \ldots (5)$$

The position of fermi level (E_F) in the two other side of heterojunction can be calculated by using the following equations [16]:

$$E_C - E_F = k_B T \ln\left(\frac{N_C}{N_D}\right) \quad \ldots (6)$$

$$E_F - E_V = k_B T \ln\left(\frac{N_V}{N_A}\right) \quad \ldots (7)$$

Where N_C and N_V are the density of states concentrations of electrons (in conduction band) and holes (valance band) respectively. The values of (E_C-E_F) and (E_F-E_V) are found to be equal 0.49 and 0.53 eV respectively. The band lineup model of SnO_2/ n-CdS/p-CdTe heterojunction was constructed depending on the yield of our data, as shown in Figure (7). Where subscripts 1 and 2 in Figure (5) correspond to CdS and CdTe respectively, and χ is the electron affinity.

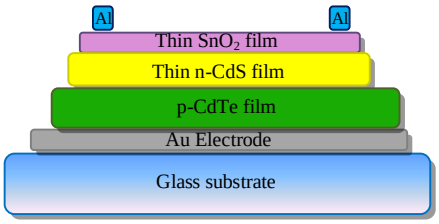

Figure (1) the typical structure of typical CdTe/CdS heterojunction.

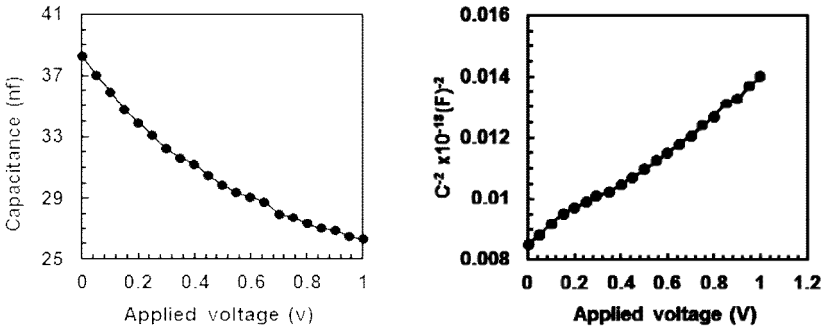

Figure (2) Mott- Shcottky plot and C-V curves SnO_2/CdS-CdTe heterojunction.

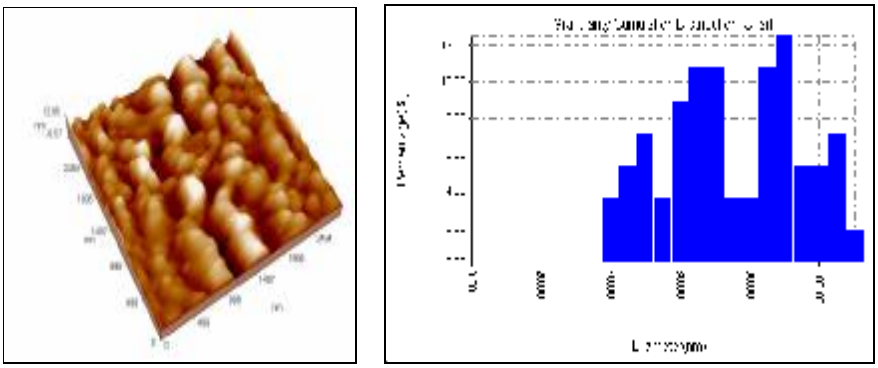

Figure (3) The Surface Morphology of SnO_2film takes from Atomic Force Microscope); the average grain size =72 nm.

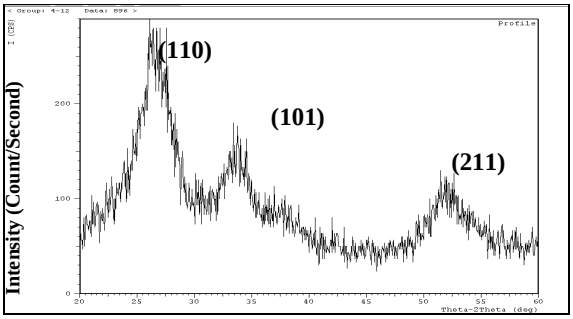

Figure (4) the X-ray diffraction pattern of SnO_2 thin film.

Table (1) the value of d for all peaks of SnO_2 thin film from X-Ray pattern.

(hkl)	(2 Ɵ) Degree	(2 Ɵ) ASTM Degree	d (XRD) (Å)	d (ASTM) (Å)
(110)	26.698	26.578	3.336	3.351
(101)	33.789	33.772	2.650	2.652
(211)	51.677	51.757	1.767	1.765

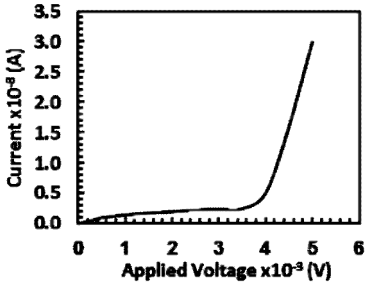

Figure (5) I-V characteristics (forward and revere bias voltage) at dark for annealed SnO_2/CdS-CdTe heterojunction.

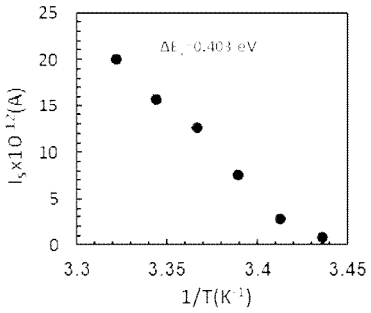

Figure (6) Saturation current vs. 10^3/T for a SnO_2/CdS-CdTe heterojunction.

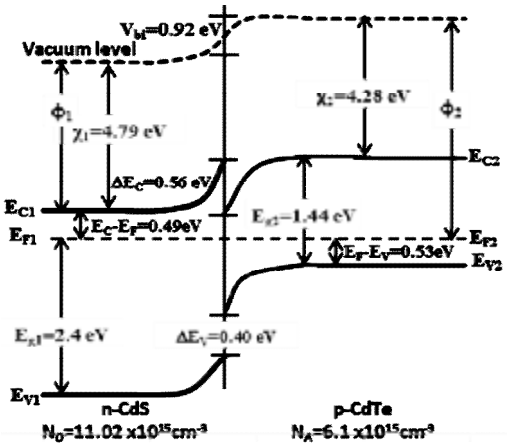

Figure (7) Equilibrium energy band (band line up) diagram of SnO_2/ n-CdS/p-CdTe heterojunction.

CONCLUSIONS

The prepared SnO_2/CdS-CdTe heterojunctions are abrupt. The Au/CdTe contact well formed. The depletion region widths, built in voltage, capacitance, and carrier concentration have been calculated. The values of doping concentration suggest that the SnO_2/CdS-CdTe interface is n^+p type. The carrier transport mechanism is tunneling – recombination. We based on our results to modified band energy diagram which has already been proposed based on the analysis of electrical measurement.

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