A New Topology of Load Network for Class F RF Power Amplifiers

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ABSTRACT

High efficiency RF power amplifiers are increasingly needed in modern mobile communication systems to reduce the battery size and power supply consumption. Class-F RF power amplifiers offer improved efficiency over the conventional class-B power amplifiers by properly controlling the harmonic components of the voltage and current signals at the output terminals of the RF device while driving it to operate as an ON/OFF switch. To do this task, a suitable load network is to be synthesized in order to present the proper harmonic impedances at the output of the RF power transistor. In this paper, a new load network for class F power amplifiers has been introduced and derived analytically. The proposed network consists of a parallel short circuited λ/8 stub, parallel open circuited λ/8 stub, and a T-section lumped-element transformer. The benefits of this topology include simplicity of design, controllable bandwidth, and harmonic tuning and impedance transformation at the same time.

To confirm the approach of analysis, a 10 W class-F UHF power amplifier circuit has been designed and simulated using a typical Gallium Nitride high electron mobility RF transistor (GaN HEMT) to operate at 500 MHz with the aid of the Advanced Design System (ADS) computer package. The simulated results have indicated that the circuit gives a dc-to-RF efficiency of more than 84 % and a power gain of 11 dB at 500 MHz with an operating bandwidth from 440 to 540 MHz.

Keywords: Class F, GaN HEMT, Load Network, RF Power Amplifier, Switching Mode PA.

INTRODUCTION

Class F RF power amplifiers are finding widespread applications in modern portable and base station transmitters due to their high-efficiency operation. The idealized operation of the class F RF power amplifier imposes the drain (or collector) voltage to be shaped as a square wave and the drain (or collector) current to be shaped as a half-wave sinusoidal waveform as shown in Figure (1) [1,2]. As seen from this sketch, there is no overlapping between the drain voltage and current waveforms, which means zero dissipated power in the RF transistor and thereby leading to 100% theoretical efficiency. If the RF device is assumed to operate as a switch then the shaping of the drain waveforms can be changed by controlling the harmonic components of the drain voltage and current through the insertion of multiple harmonic resonators in the output matching (or load) network of the power amplifier. These resonators must present open circuit (harmonic peaking) to the odd harmonic components and short circuit (harmonic termination) to the even harmonic components at the device output [3]. Accordingly, the drain to source voltage at the device output contains only odd harmonics while the drain current contains only even harmonics. In other words, the input impedance of the drain network represents an open circuit to the odd harmonics and a short circuit to the even harmonics.

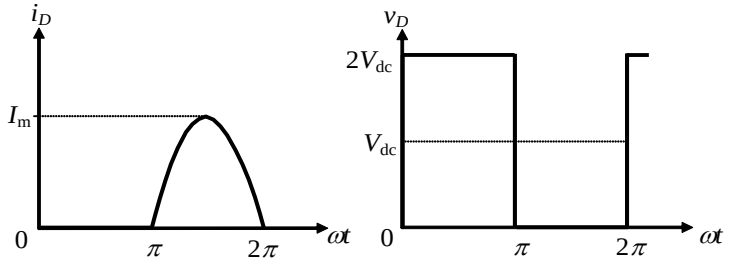

Figure (1): Idealized Waveforms of the Drain Current and Voltage in the Class F Power Amplifier.

The drain voltage of Figure (1) can be generally described as [4]:

$$v_D(\omega t) = V_{dc} + V_{d1}\sin(\omega t) + \sum_{n=3,5,7,\ldots}^{\infty} V_{dn}\sin(n\omega t) \quad \ldots..(1)$$

where V_{dc} represents the dc voltage at the drain, V_{d1} is the amplitude of the fundamental component of the drain voltage and V_{dn} is the amplitude of the n^{th} odd harmonic component of the drain voltage.

Similarly, the drain current waveform can be written in the form [4]:

$$i_D(\omega t) = I_{dc} - I_{d1}\sin(\omega t) - \sum_{n=2,4,6,\ldots}^{\infty} I_{dn}\cos(n\omega t) \quad \ldots\ldots (2)$$

where I_{dc} is the dc component of the drain current, I_{d1} is the amplitude of the fundamental component of the drain current and I_{dn} is the amplitude of the n^{th} even harmonic component of the drain current.

Equations (1) and (2) imply that there is a phase shift of 180^o between the fundamental components of the drain voltage and current.

Using Fourier series expansion, it can be proved that:

$$V_{dc} = V_{dd} \quad \ldots\ldots (3)$$

$$V_{d1} = \frac{4V_{dd}}{\pi} \quad \ldots..(4)$$

$$I_{dc} = \frac{I_m}{\pi} \quad \ldots..(5)$$

$$I_{d1} = \frac{I_m}{2} \quad \ldots..(6)$$

where V_{dd} is the drain supply voltage, and I_m is the maximum or peak drain current of the RF transistor.

The drain impedance at the fundamental frequency can be defined as:

$$Z_{d1} = -\frac{V_{d1}}{I_{d1}} \quad \ldots..(7)$$

Substituting equations (4) and (6) in equation (7) yields:

$$Z_{d1} = R_{opt} = \frac{8}{\pi}\frac{V_{dd}}{I_m} \quad \ldots..(8)$$

where R_{opt} is the optimum load line resistance for the class F mode of operation.

The maximum drain current, I_m, can be determined from the RF device specifications or from the simulated drain dc characteristics.

In order to avoid distorting the drain current pulse, the drain voltage should not swing below the knee or saturation voltage and therefore equation (8) is modified to be [5]:

$$R_{opt} = \frac{8}{\pi}\frac{(V_{dd} - V_{sat})}{I_m} \quad \ldots..(9)$$

where V_{sat} is the drain-to-source saturation (or knee) voltage.

The necessary conditions for the input impedance of the load network at the drain of the RF transistor are thus:

$$Z_d = \begin{cases} R_{opt} & at\ fundamental\ frequency \\ 0 & for\ even\ harmonics \\ \infty & for\ odd\ harmonics \end{cases} \quad \ldots\ldots(10)$$

The conventional class F switching mode RF power amplifier circuit is presented in Figure (2) [6]. The input signal is assumed to be a square wave to drive the RF transistor into saturation and cut-off regions consequently. In this circuit the load network consists of a λ/4 transmission line section and a parallel tank circuit tuned at the fundamental frequency. The tank circuit presents high impedance (ideally open circuit) at the fundamental frequency and a short circuit at all other harmonic frequencies. Therefore the transmission line transformer acts ideally as a short circuited λ/4 stub at all the harmonic frequencies other than the fundamental one. So, it presents a repetitive short circuit at the even harmonics, and a repetitive open circuit at odd harmonics while transforming the load resistance, R_L, into the optimum class F load line resistance at the fundamental frequency.

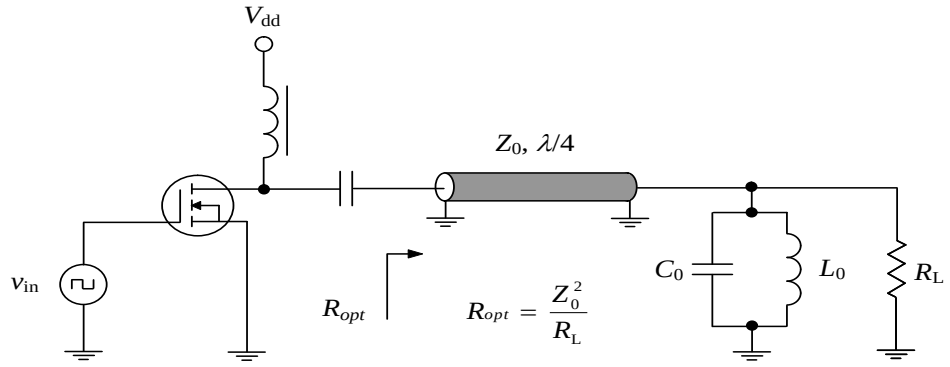

Figure (2): Schematic Diagram of the Conventional Class F RF Power Amplifier.

A unified method for designing loading networks for class F switching mode power amplifiers using lumped elements was documented [7]. In this technique, the loading networks are synthesized to present infinite impedance at the fundamental frequency and its third harmonic, and low impedance to ground at the second harmonic. A similar approach was reported with new types of loading networks of class F power amplifiers using both lumped and distributed elements [8]. In this approach, explicit-form expressions were derived to evaluate each circuit element in the loading network. However, in these techniques a separate matching network should be added to present the proper load impedance at the fundamental frequency. Besides, these methods are primarily targeted toward narrowband tuned class F power amplifiers. Another design technique was adopted for both class F and inverse class F power amplifier loading networks using embedded low pass filter sections [9]. In this method, the RF transistor's lead inductance and output capacitance are considered as part of the loading network. However, the element values of the load network are difficult to be evaluated analytically and require computer optimization. Chebyshev bandpass filters are also used to realize the load networks of class F RF power amplifiers to achieve matching and harmonic tuning at the same time [10]. Unfortunately, the latter technique is somewhat complicated and requires extensive calculations.

Topology of The Load Network

The load network of the conventional class F RF power amplifier must present an open circuit at odd harmonic frequencies and a short circuit at even harmonics while presenting the required load line resistance at the fundamental signal frequency. Figure (3) shows a generalized block diagram of the proposed load network.

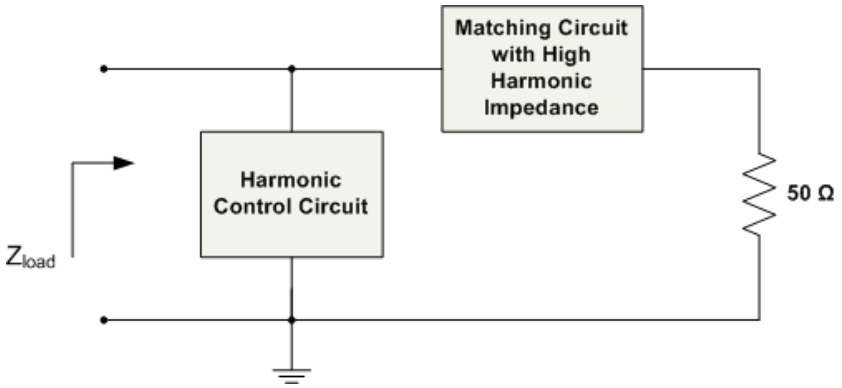

Figure (3): General Topology of the Load Network.

The input impedance of the load network, Z_{load}, should satisfy the conditions of Z_d given in equation (10). The harmonic control circuit, sometimes called the impedance peaking circuit, is synthesized to terminate the second harmonic frequencies and to maximize the odd harmonics of the voltage waveform. The matching circuit, on the other hand, is designed to transform the 50 Ω load resistance into the required optimum resistance for class F operation at the fundamental frequency while giving high impedance at all other harmonic frequencies. The high impedance of the matching circuit is necessary to avoid loading the harmonic control circuit at the harmonic frequencies which may otherwise cause shifting in the frequency response of this circuit. The bandwidth of the matching circuit depends on its quality factor which can be taken as a parameter in the synthesis process.

In conventional class F power amplifiers, the λ/4 short-circuited transmission line is used to control the harmonics at the drain of the RF transistor. In this work, a new impedance peaking network is introduced as shown in Figure (4). It consists of two parallel open-circuited and short-circuited λ/8 stubs having the same characteristic impedance, Z_o.

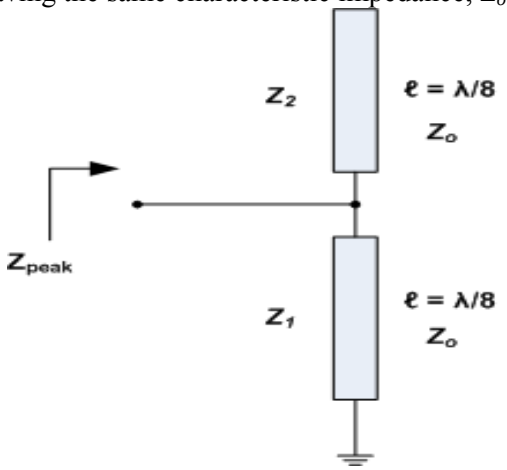

Figure (4): Impedance Peaking Circuit.

The input impedance of the shorted transmission line can be expressed by [11]:

$$Z_1 = jZ_o \tan(\theta) \quad \ldots\ldots (11)$$

On the other hand, the input impedance of the open stub is given by [11]:

$$Z_2 = -jZ_o \cot(\theta) \quad \ldots\ldots (12)$$

where θ is the electrical length of the two transmission lines.

The input impedance of the peaking network, Z_{peak}, is the parallel combination of Z_1 and Z_2:

$$Z_{peak} = \frac{Z_1 . Z_2}{Z_1 + Z_2} = \frac{jZ_o}{\cot\theta - \tan\theta} \quad \ldots\ldots (13)$$

After some arrangement, equation (13) can be expressed as:

$$Z_{peak} = \frac{jZ_o \tan\theta}{1 - \tan^2\theta} \quad \ldots\ldots (14)$$

Recalling that:

$$\tan(2\alpha) = \frac{2\tan\alpha}{1 - \tan^2\alpha} \quad \ldots\ldots (15)$$

Thus, equation (14) can be simplified to:

$$Z_{peak} = \frac{1}{2} jZ_o \tan(2\theta) \quad \ldots\ldots (16)$$

Z_{peak} can be expressed as a function of frequency by substituting $\theta = \beta\ell$, where β is the phase constant which is given by $2\pi/\lambda$ and $\ell = \lambda_o/8$, where λ_o represents the wavelength at the fundamental frequency component. Based on these facts, Z_{peak} can be written as:

$$Z_{peak}(f) = \frac{1}{2} jZ_o \tan\left(\frac{\pi}{2} . \frac{f}{f_o}\right) \quad \ldots\ldots (17)$$

where f_o is the fundamental frequency of the RF signal.

Equation (17) reveals that the equivalent impedance of the harmonic control network is similar to that of the conventional $\lambda/4$ short-circuited stub but with a multiplication factor of 0.5. This will sharpen the response around the poles and zeros of the impedance function, and give better harmonic peaking and termination characteristics.

In Figure (5), the magnitude of the input impedance of the harmonic peaking circuit is compared with that of the $\lambda/4$ short-circuited stub with a frequency sweep from 0 to 2.6 GHz at a fundamental frequency f_o of 500 MHz. As shown from this sketch, the impedance response of suggested peaking circuit is narrower around the odd harmonic frequencies. This will give additional reduction of the signals at frequencies around the harmonics of the fundamental frequency.

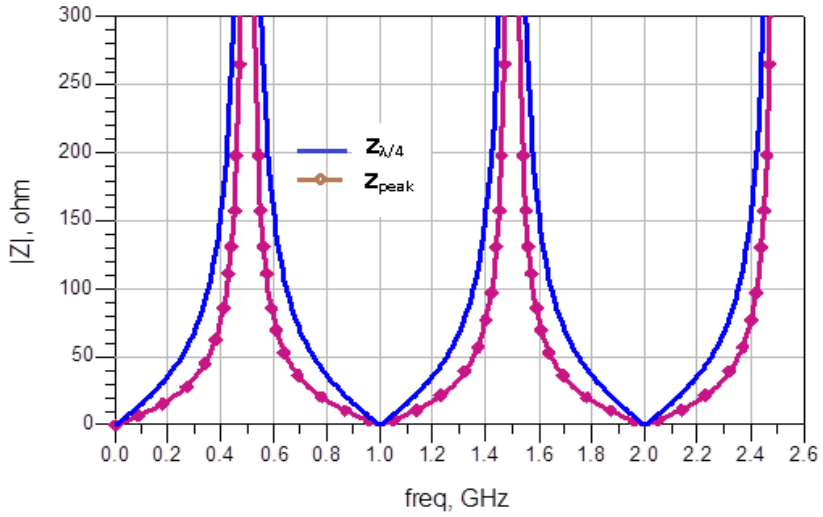

Figure (5): Impedance Response of the Suggested Harmonic Peaking Circuit Compared with that of the Shorted $\lambda/4$ Transmission Line.

The matching network appearing in Figure (3) can be synthesized to transform the 50 Ω load impedance into the optimum load-line resistance, R_{opt}, at the fundamental frequency. It should also present high impedance to the harmonic frequency components so that not to load the harmonic peaking circuit at these frequencies. The quality factor of the matching circuit can also control the bandwidth of the amplifier circuit. Based on these facts, the T-Section circuit shown in Figure (6) can be taken to fulfill the desired requirements. The two inductors, L_1 and L_2, give high reactive impedance at the harmonic frequencies.

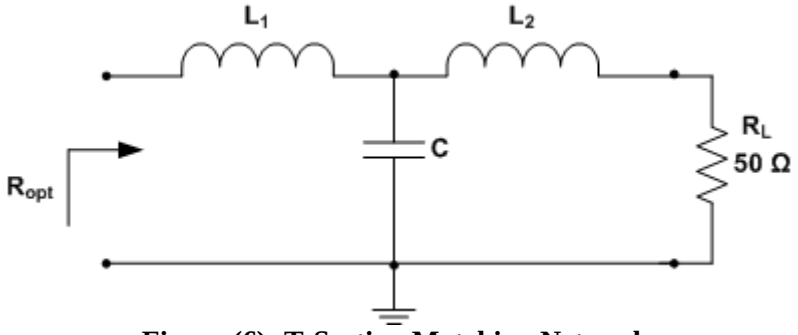

Figure (6): T-Section Matching Network.

The element values of the T-section matching circuit can be determined after selecting the required Q-factor as follows [12]:

$$A = \sqrt{\frac{R_{opt}}{R_L}(1+Q^2) - 1} \qquad \ldots..(18)$$

$$L_1 = \frac{Q.R_{opt}}{2\pi f_o} \qquad \ldots..(19)$$

$$L_2 = \frac{A.R_L}{2\pi f_o} \qquad \ldots..(20)$$

$$C = \frac{Q + A}{2\pi f_o.R_{opt}(1+Q^2)} \qquad \ldots..(21)$$

where f_o is the fundamental frequency of operation, A is a calculated constant, and R_L = 50 Ω.

Alternatively, the element values of the matching circuit can be determined graphically using Smith chart with the aid of the constant Q-circle. The topology of the load network will thus be as presented in Figure (7). The T-section matching circuit may however load the harmonic peaking circuit at the odd harmonic frequencies which may cause a slight shift in the impedance peaking points around these frequencies. This frequency shift is mainly dependent on the Q-factor of the matching circuit. The higher the Q, the lower is the shift in the harmonic frequencies.

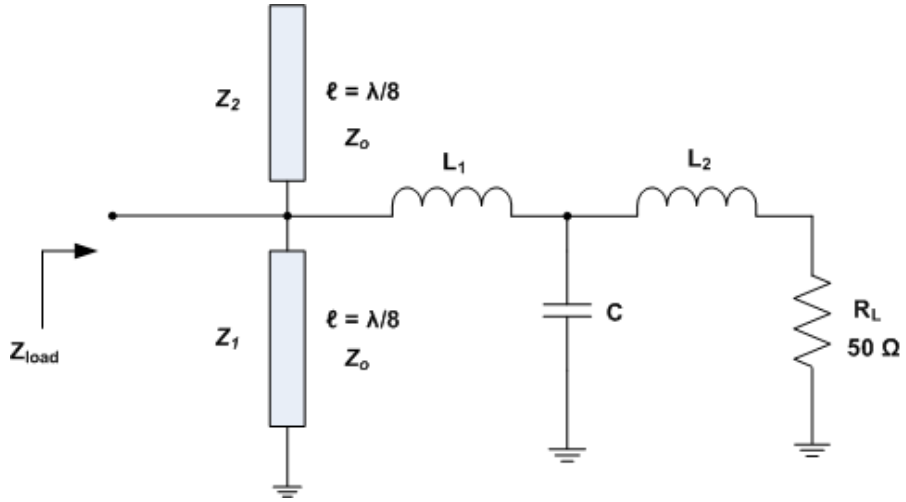

Figure (7): Configuration of the Proposed Load Network.

Design of A 10 W Uhf Power Amplifier Circuit

In order to confirm the validity of the proposed load network, a class-F power amplifier circuit is to be designed at an operating frequency of 500 MHz. In this design the modern gallium nitride (GaN) high electron mobility transistor (HEMT) CGH40010 of Cree, Inc. has been selected. This device operates from a 28 V DC supply and can deliver more than 10 W output RF power up to 4 GHz. This transistor offers also high power gain and broadband operation. The high operating voltage of the GaN HEMT semiconductor technology stems from its relatively high band-gap energy and the corresponding high breakdown electric field. Besides, the high power density offered by the GaN technology allows millimeter size devices with several watts of output power level to be fabricated [13].

The transfer characteristic of the CGH40010 GaN HEMT RF power transistor is simulated in Figure (8) using the SPICE large signal model of this device. This sketch shows that the threshold gate-to-source voltage equals to -2.5 V approximately. This value of V_{GS} is taken as the Q-point of the class F mode of operation. In Figure (9), the drain characteristic of the RF transistor is presented. As shown from Figure (9), the drain-to-source saturation (or knee) voltage is relatively high and is in the order of 4 V. The maximum allowable drain current for this device is specified by the manufacturer's datasheet to be 1.5 A. Hence, the optimum load line drain resistance at the fundamental frequency, R_{opt}, is calculated from equation (9) to be 40 Ω.

To design the load network, the *Q*-factor of the matching circuit should first be determined. It actually depends on the desired bandwidth of power amplifier circuit and can be estimated from:

$$Q = \frac{f_o}{BW} \qquad \ldots\ldots (22)$$

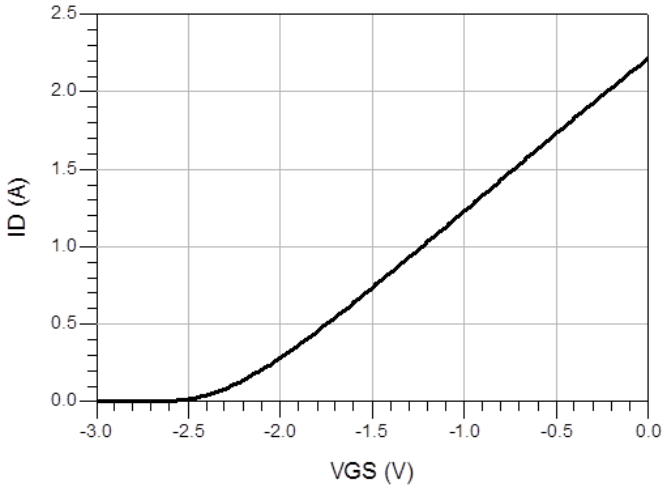

Figure (8): Drain Current versus Gate Voltage for the GaN HEMT Transistor.

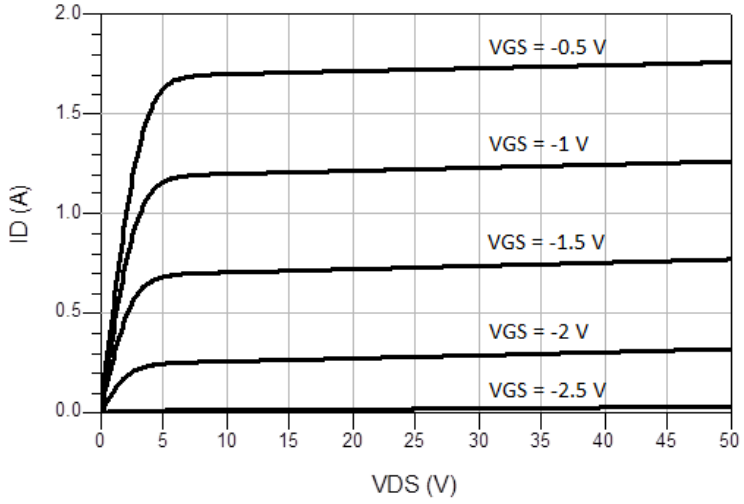

Figure (9): Drain Current versus Drain-to-Source Voltage.

Since the operating frequency of the circuit, f_o, is 500 MHz, therefore the Q-factor equals to 5 for a desired bandwidth, BW, of 100 MHz. Practically, the Q-factor should be selected to be less than the calculated value in order to account for the parasitic elements of the circuit which may decrease the overall bandwidth.

The circuit elements of the matching network are calculated from equations (18-21) to transform the 50 Ω impedance into 40 Ω (R_{opt}) at the fundamental frequency for the given Q-factor. For a value of Q = 2, the element values are L_1 = 25 nH, L_2 = 27 nH, and C = 6 pF. In Fig. 10, the impedance response of the load network in Figure (7) is presented for two values of quality factor. Although the two circuits present the same impedance (40 Ω) at the fundamental frequency, there is a slight shift in the response at the third harmonic frequency (1.5 GHz). When Q = 5, the load network presents a third harmonic impedance of 556 Ω, while it is reduced to 216 Ω when the quality factor is 2. However, the load network gives wider bandwidth when Q = 2.

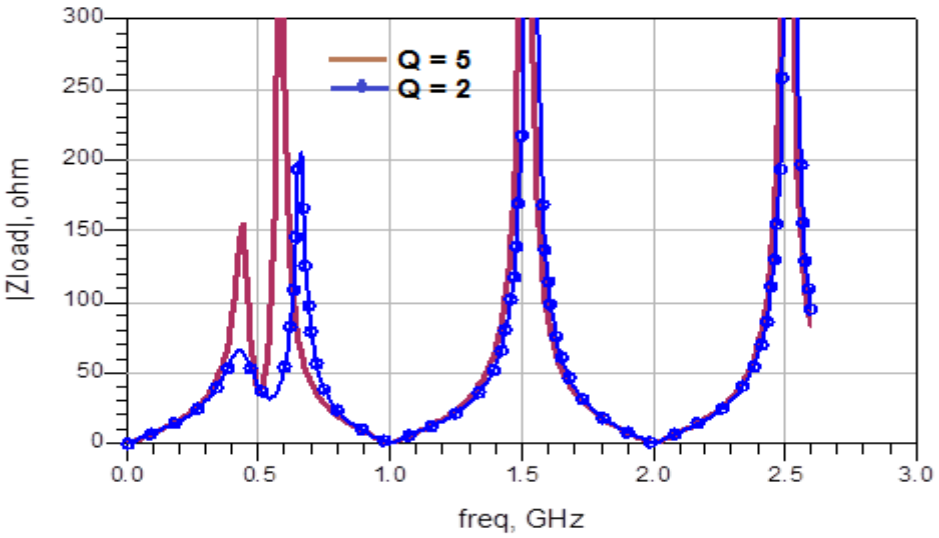

Figure (10): Impedance Response of the Load Network with Different Quality Factors.

The block diagram of the class-F RF power amplifier is shown in Figure (11). The input matching network is designed to match the large signal input impedance at the gate terminal of the HEMT transistor with the 50 Ω system impedance. The stability network is a resistive (lossy) circuit used to prevent any tendency to oscillation and to increase the stability factor of the amplifier [14].

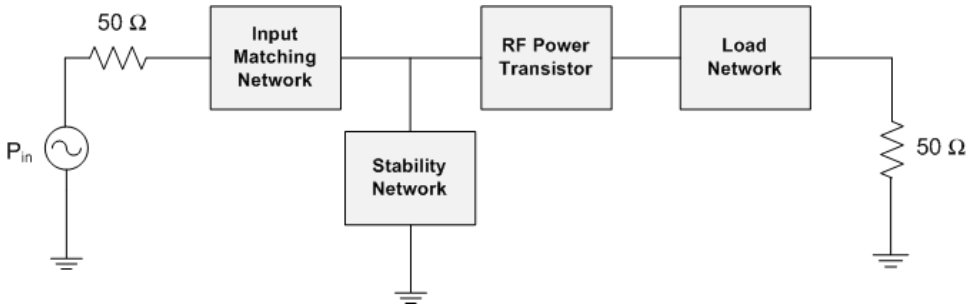

Figure (11): Block Diagram of the RF Power Amplifier.

In order to design the input matching network, the input impedance of the RF power device should first be evaluated over the desired bandwidth with the load and stability networks inserted in the amplifier circuit. Figure (12) presents a schematic diagram of the power amplifier circuit without the input matching network. The transmission line sections are implemented as two microstrip lines using FR-4 substrate with a dielectric constant of 4.5 and a board thickness of 1.6 mm. The drain supply voltage is delivered to the HEMT transistor through the short-circuited stub of the load network, which is in turn connected to RF ground via a 470 pF bypass capacitor. The HEMT transistor is biased at the threshold gate-to-source voltage to place the RF device at the edge of the cut-off region. Resistor R_1 and inductor L_3 represent the stability network to ensure stabilized amplifier operation over the desired band. The values of R_1 and L_3 have been optimized using ADS simulation capabilities. The circuit is analyzed using the harmonic-balance algorithm to evaluate the input impedance at the gate of the transistor over the frequency band from 440 MHz to 540 MHz with the input RF power set to 1 W.

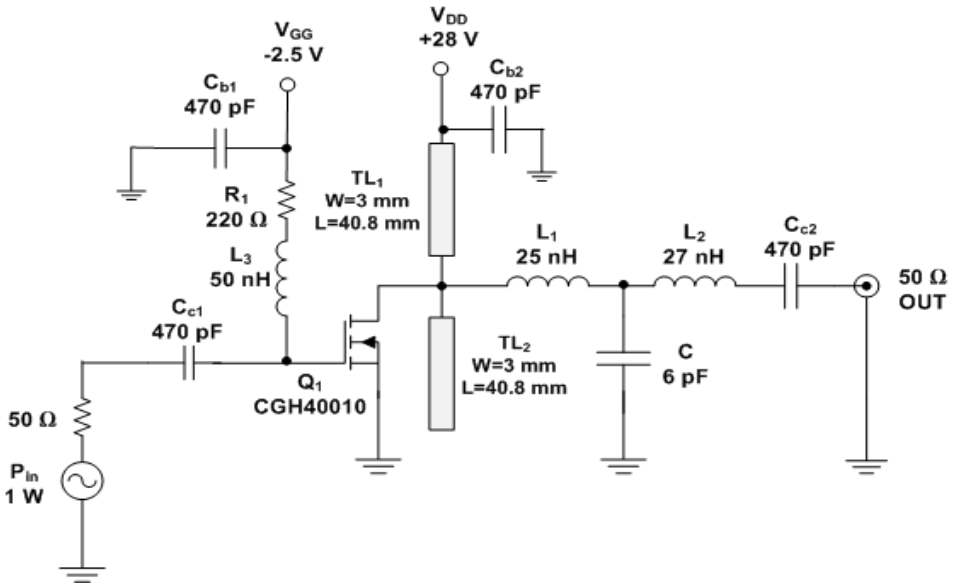

Figure (12): Circuit Schematic of the Class F Power Amplifier without the Input Matching Network.

The input impedance at the gate terminal of the HEMT transistor is presented in Figure (13) across the frequency band of interest. This sketch indicates that the gate impedance is capacitive with a value of Z_g = 11-j46 Ω approximately at 500 MHz. An input matching network is hence needed to transform the gate impedance into 50 Ω in order to minimize the input voltage standing wave ratio (VSWR) of the overall power amplifier circuit. With the aid of the Smith chart, a matching circuit consisting of a series inductor with a value of 23 nH and a parallel capacitor of 8.2 pF is synthesized for this purpose. The schematic diagram of the overall power amplifier circuit is presented in Figure (14).

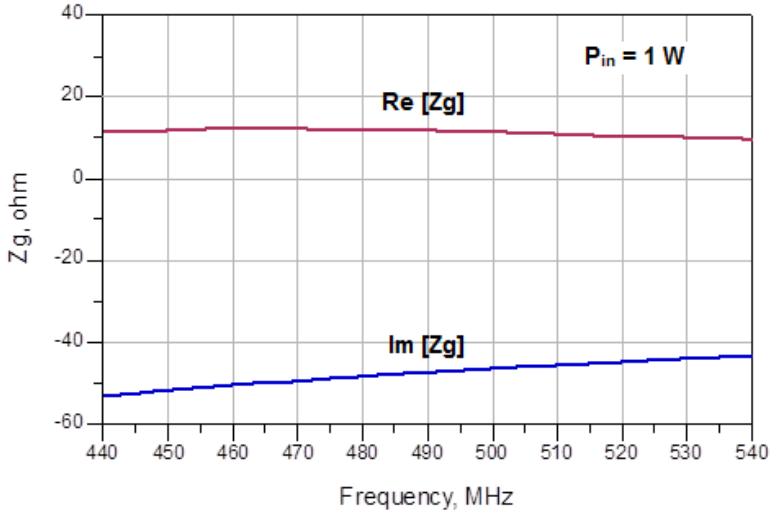

Figure (13): Simulated Gate Impedance versus Frequency.

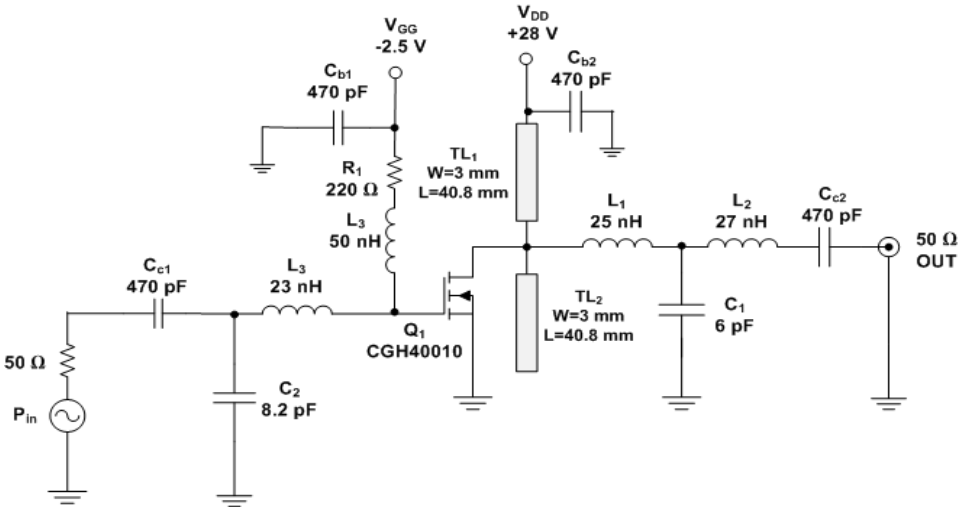

Figure (14): Schematic Diagram of the Designed Class F Power Amplifier.

Simulation Results

The designed power amplifier circuit of Figure (14) has been simulated with the aid of the harmonic balance simulator of the ADS software package. Figure (15) presents the drain voltage waveform of the HEMT transistor, while Fig. 16 shows its drain current waveform at 500 MHz with an input power level of 1 W. The simulated drain voltage waveform looks like a semi-square wave when compared with the ideal waveform of Figure (1). This waveform is shaped by the response of the load network in addition to the nonlinear output capacitance and lead inductance of the RF power device. The drain current waveform of Figure (16) is an approximation of the half-wave sinusoidal pulses and seems to be out of phase with the drain voltage waveform with minimum overlapping. This non-overlapping behavior reduces the power dissipation in the drain of the HEMT transistor and increases power amplifier's efficiency.

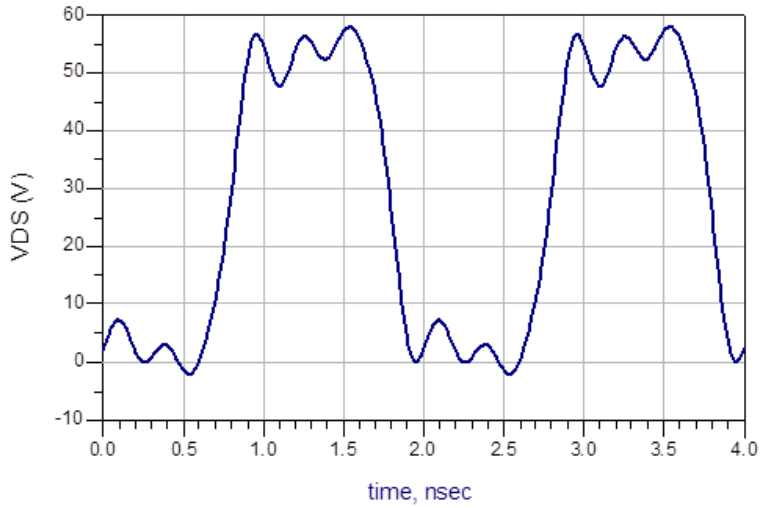

Figure (15): Simulated Drain Voltage Waveform at 500 MHz.

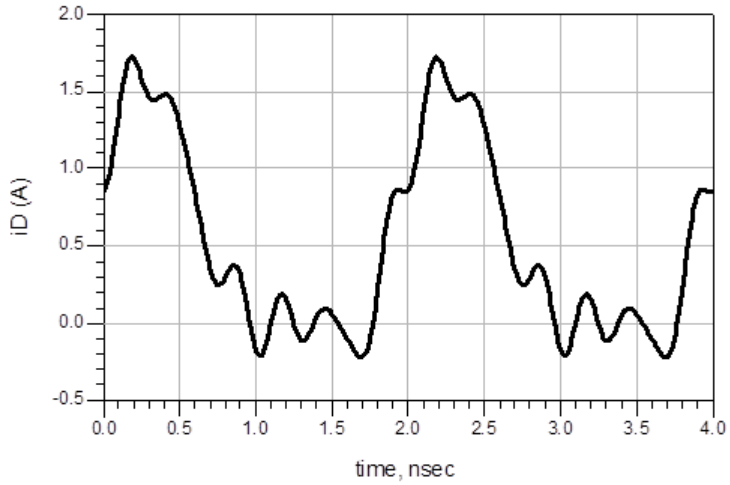

Figure (16): Simulated Drain Current Waveform at 500 MHz.

In Figure (17), the output voltage waveform of the power amplifier circuit is sketched. The sinusoidal nature of this waveform is referred to the low-pass filtering effect of the output matching network in minimizing the amplitudes of the harmonic components.

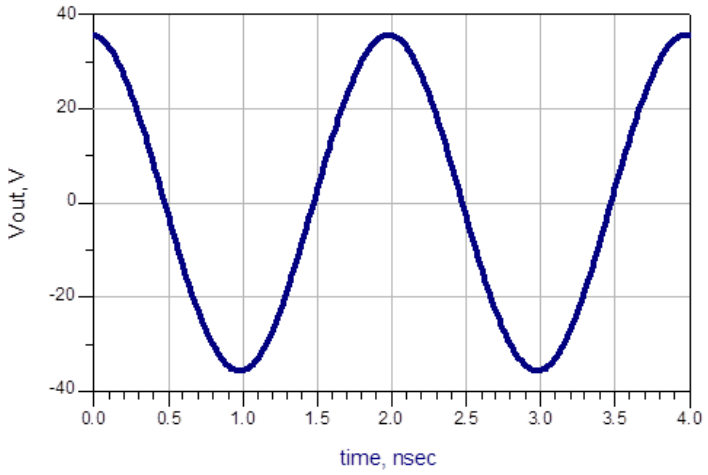

Figure (17): Simulated Output Voltage Signal at 500 MHz.

In Figure (18), the output power is sketched against input power level in dBm with a simulation frequency of 500 MHz. It is shown that the amplifier delivers more than +40 dBm (10 W) at input power level of 30 dBm (1 W). It can be seen from this sketch that the RF device goes deeply into saturation at this power level. The power gain of the amplifier circuit is presented in Figure (19), being about 11 dB at input power level of 30 dBm. The 1-dB gain compression point occurs at an input power of 15 dBm with the power gain falling rapidly after this point.

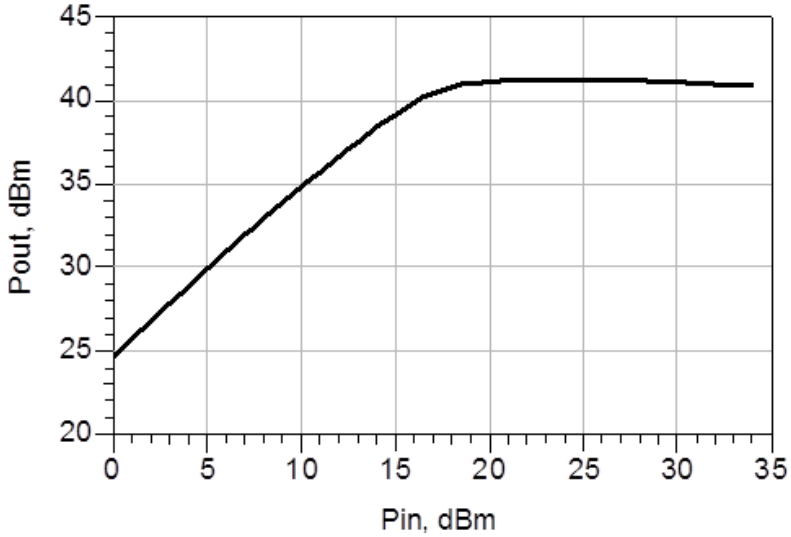

Figure (18): Output Power versus Input Power.

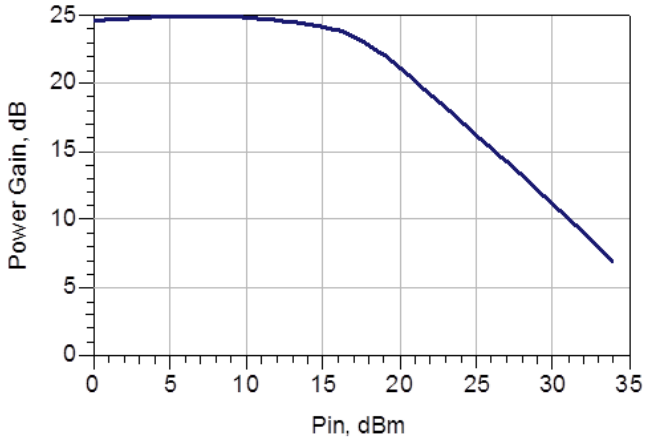

Figure (19): Simulated Power Gain versus Input Power.

The drain efficiency of the power amplifier is sketched in Figure (20) together with the power-added efficiency (PAE). It is shown that the circuit possesses a drain efficiency of 84.8 % and a power added efficiency of 78.2 % at input power level of 1 W. The drain efficiency, also known as the dc-to-RF efficiency, is calculated from:

$$\eta_D = \frac{P_{out}}{P_{dc}} \times 100 \quad \ldots\ldots (23)$$

where P_{out} is the output RF power, and P_{dc} is the dc delivered power given by:

$$P_{dc} = V_{dd} . I_{dc} \quad \ldots\ldots (24)$$

V_{dd} represents the drain supply voltage and I_{dc} is the dc component of the drain current.
On the other hand, the power added efficiency of the circuit is calculated from:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \times 100 \quad \ldots\ldots (25)$$

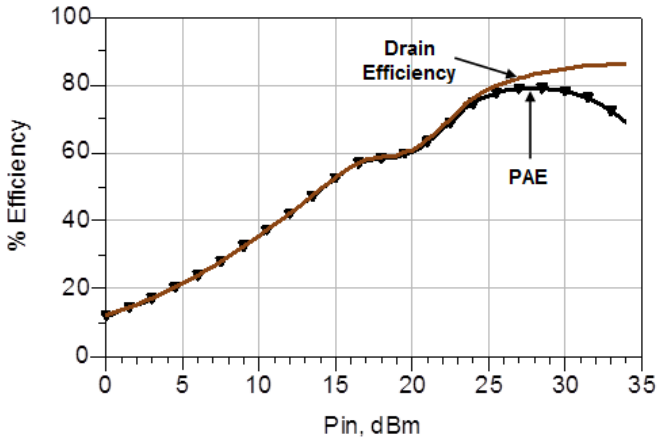

Figure (20): Efficiency versus Input Power.

The circuit has then been simulated over a frequency band from 440 MHz to 540 MHz with the input power maintained at 1 W. Figure (21) presents the power gain of the amplifier versus frequency. It is shown that the power gain is about 10±1 dB over the entire band. In Figure (22), the output power is sketched with frequency, while Figure (23) displays the drain efficiency and power added efficiency of the circuit. The power amplifier circuit gives a dc to RF efficiency of more than 80 %, and a power-added efficiency of more than 75 % all over the band. Finally, the input return loss is displayed in Figure (24) showing an acceptable match over the frequency band of interest.

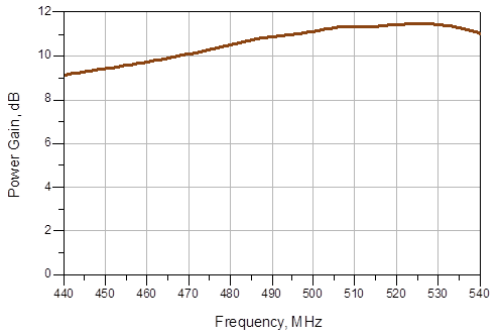

Figure (21): Power Gain versus Frequency.

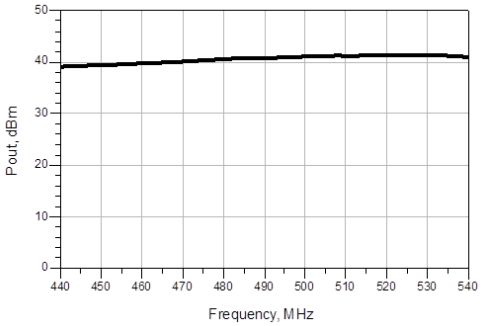

Figure (22): Output Power versus Frequency.

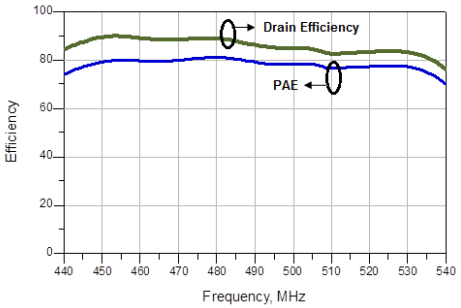

Figure (23): Efficiency versus Frequency.

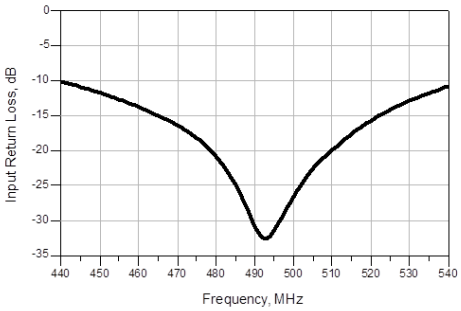

Figure (24): Input Return Loss versus Frequency.

CONCLUSION

A load network topology for class F switching mode RF power amplifiers has been proposed and analyzed. The main features of the network are its simplicity of construction, controllable bandwidth, and predictable behavior. The proposed network has been verified through a design process of a 10 W class F power amplifier operating within the frequency band 440-540 MHz using a modern HEMT RF power transistor. The simulation results show that a drain efficiency of more than 84 % has been obtained at 500 MHz with a power gain of 11 dB at the nominated output power level. Although this network consists of both lumped and distributed elements, it can be modified to be constructed solely of distributed elements (microstrip lines) by replacing the T-section matching circuit with an equivalent transmission-line network. This may increase the operating frequency of the circuit into the giga-hertz range. It has been verified also that broadband power amplifier response can be obtained with careful design using the proposed network topology.

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