IMPLEMENTATIONS OF 8×8 DCT AND IDCT ON DIFFERENT FPGA TECHNOLOGIES USING THE MODIFIED LOEFFLER ALGORITHM

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ABSTRACT
In this paper the hardware implementations is investing of 8x8 Discrete Cosine Transform (DCT) and Inverse Discrete Cosine Transform (IDCT) on different Field Programmable Gate Array (FPGA) technologies using the modified Loeffler algorithm. The investigations involved simulations and synthesis of Very High Speed Integrated Circuit Hardware Description Language (VHDL) code utilizing recent FPGA families of Xilinx, Altera, and Lucent. The paper achieving the most demanding real-time requirements of some standardized frame resolutions and rates. Synthesis results for 8-point DCT/IDCT implementations indicate operating frequencies of 50 MHz, 60 MHz, and 22 MHz for the investigated Xilinx, Altera and Lucent FPGA chips, respectively. These frequencies allow 2193 Source Input Format (SIF) and 100 High Definition Television (HDTV) frames to be processed by the Xilinx FPGA. The resulting frame processing rates for Altera are 877 and 40 for SIF and HDTV, while for Altera they are 647 and 29, respectively. Results indicate that the investigated FPGA implementations would speed DCT based compression algorithms up to frame rates well above the real-time requirements of SIF, International Consulting Committee on Radio & Television (CCIR-TV) and HDTV frame formats.

الخلاصة
في هذه المنشورة تم الاستقصاء عن البناء المادي ل8×8 تحويلة الجيب تمام المنتقعة (DCT) وتعكسة (IDCT) باستخدام أجهزة FPGA المتطورة (VHDL) في فترة زمنية لوحدها لترجمة الورقة复 لذات الكيان المادي ذات السرعة العالية جدا (VHDL) المستخدمة في الأونة الأخيرة عن طريق مثال ترتيب براءة برمجة المجال للمجال لمصلحة Lucent & Xilinx Altera من شركة (FPGA). ان ترتيب ترتيبات الزمن الحقيقي (real-time) لبعض ترتيبات اليات المعمولة النصية لبرمجة المجال.Lucent & Xilinx Altera من شركة (FPGA). ترتيب تركيب لبناء 8 نقط ترتيبة جيدا المتطورة (DCT) أو مكونياتها نسبه إنه ترددات العمل هي 50 ميغاهرتز و22 ميغاهرتز، 60 ميغاهرتز و22 ميغاهرتز لقطع ترتيب براة المجال على التولي. النتائج تبين أنه استخدام البناء DCT & IDCT لبايعك الاقتراب يكون أكثر من تحقيق متطلبات الزمن الحقيقي.
Introduction

Discrete cosine transform (DCT) and inverse discrete cosine transform (IDCT) are widely used in video coding and image processing standards. The decorrelation and energy compaction properties of the transform have been exploited to achieve high compression ratios in MPEG and JPEG. The N-point 1-D DCT is defined by [Rao 1990]:

\[ \text{DCT} = \frac{1}{\sqrt{N}} \sum_{n=0}^{N-1} x(n) \cos \left( \frac{\pi}{N} kn \right), \quad k = 0, \ldots, N-1 \]

The remainder of the paper is organized as follows. It is briefly described in Background some synthesis and simulation results prove that the investigated FPGA implementations can speed up DCT to frame rates well above the real-time requirements of CIF, CCIR-601, and HDTV standards. The methodology of the experimentation and the detailed hardware implementation are presented in last Section. Finally, concluding remarks are presented in last Section.

Keywords

DISCRETE COSINE TRANSFORM (DCT); VITAL: FPGA; RECONFIGURABLE PROCESSOR.

Implementations of 8 x 8 DCT and IDCT on different FPGA Technologies Using the Modified Loeffler Algorithm

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Where $X(k) =$ The $N$-point 1-D DCT.

And $Y(n) =$ The $N$-point 1-D IDCT is defined by:

$$
Y(n) = \frac{2}{N} \sum_{k=0}^{N-1} c_k X(k) \cos \left[ \frac{(2n-1)k\pi}{2N} \right], \quad n = 0, 1, \ldots, N-1
$$

(2)

where $c_k = \begin{cases} 
1; & k = 0 \\
\sqrt{\frac{2}{N}}; & k \neq 0 
\end{cases}$

DCT and IDCT are highly computational intensive, which creates prerequisites for performance bottlenecks in systems utilizing them. To overcome this problem, a number of algorithms have been proposed for more efficient computations of these transforms. 8-point is used 1-D DCT/IDCT algorithm in all experiments, proposed by van Eijndhoven and Sijstermans [Van 1999]. This algorithm is a slight modification of the original Loeffler algorithm [Loeffler 1989], which provides one of the most computationally efficient 1-D DCT/IDCT calculations. The modified Loeffler algorithm for calculating 8-point 1-D IDCT is illustrated in Fig. (1).

![Fig. (1). The 8-point IDCT - modified Loeffler algorithm](image)

The round block in Figure 1 signifies a multiplication by $\sqrt{\frac{1}{2}}$. The butterfly block it is presented in Fig. (2).

![Fig. (2). The Butterfly](image)
Where:

\[ O_0 = I_0 - I_1 \]  \hspace{1cm} (3)
\[ O_1 = I_0 - I_1 \]  \hspace{1cm} (4)

The rectangular block depicts a rotation, which transforms a pair of inputs \([I_0, I_1]\) into outputs \([O_0, O_1]\). The symbol is depicted in Fig. (3).

![Fig. (3). The rotator](image)

\[ O_0 = I_0 \cos \left( \frac{n \pi}{16} \right) - I_1 \sin \left( \frac{n \pi}{16} \right) = C \cdot I_0 - S \cdot I_1 \] \hspace{1cm} (5)
\[ O_1 = I_0 \sin \left( \frac{n \pi}{16} \right) + I_1 \cos \left( \frac{n \pi}{16} \right) = S \cdot I_0 + C \cdot I_1 \] \hspace{1cm} (6)

The implementation of the rotator depicted in Fig. (4) utilizes four multipliers and two adders to shorten critical path and improve numerical accuracy. This direct implementation has been proven to be ideal for fixed-point arithmetic [Sim 2001]. Indeed, some other implementations of the rotator are possible, e.g., with three multipliers and three adders. These alternative designs, however, have longer critical paths and involve initial additions, which may lead to overflows and may affect the accuracy of the calculations [Babic 2003].

![Fig. (4). Implementation of the rotator for IDCT](image)
The algorithm is depicted of 8-point DCT in Fig. (5).

![Diagram of 8-point DCT](image)

Fig. (5). The 8-point DCT - modified Loeffler algorithm

The functionality of the rotator in DCT is slightly different than in IDCT, while the round block and the butterfly are exactly the same [Cho 1991].

The DCT rotator block equations are:

\[
O_0 = I_0 \cos \frac{n\pi}{16} - I_1 \sin \frac{n\pi}{16} = C^* I_0 - S^* I_1
\]

(7)

\[
O_1 = -I_0 \sin \frac{n\pi}{16} - I_1 \cos \frac{n\pi}{16} = -S^* I_0 + C^* I_1
\]

(8)

In video data compression standards, the 2-D DCT/IDCT is defined. One possible approach to compute the 2-D DCT/IDCT is the standard row-column separation. In this approach, the 1-D transform is applied to each row [Cho 1991], & [Ren 1998]. On each column of the result 1-D transform is performed again, to produce the final result of the 2-D DCT/IDCT. In our experiments we use this strategy.

**METHODOLOGY OF THE IMPLEMENTATION**

All experiments involve processing video data with different frame formats. It will have chosen the SIF, CCIR-TV and the HDTV formats, since they have been considered by many video compression standards. The frame resolutions for SIF, CCIR-TV and HDTV are 352x288, 525x720 and 1152x1926, respectively. It is written synthesizable VHDL models of two units, one describing 1-D DCT and the other – 1-D IDCT. The designs have been implemented according to the modified
Loeffler algorithm. Both simulated and synthesized the VHDL models for three different FPGA technologies, namely Virtex II, Aecx-1K and Orea using the following design tools:

1- ModelSim SE/EE from Model Technology, version 54.b, revision 2000.06, for simulating the VHDL source code;
2- LeonardoSpectrum from Exemplar, version v2000.1a2.75, for the synthesis of VHDL source code.

8-bit is considered input data to design DCT for consistency with the 8-bit color presentation in visual data compression standards like MPEG and JPEG. The output data width was designed to be 10-bit. Similarly, 10-bit inputs and 8-bit outputs were considered for the IDCT design. The row-column separation strategy was used to compute the 2-D DCT/IDCT. As it have used 8-point 1-D DCT and IDCT, the FPGA I/O ports delay, reported by the synthesis software, is in essence the data processing delay for 8 pixels. Implementing matrix transposition without extra delay, can multiply the 8point 1-D DCT I/O latency by 16 to calculate the latency of the 8x8 DCT transform. This is in essence the processing latency for one 8x8 pixel block. Given this latency, it can easily calculate the time, required to transform all 8x8 blocks in any video frame for the selected formats - SIF, CCIR- TV and HDTV. Frame processing rate (frames per second) of the implemented DCT/IDCT was the main criterion used to estimate and compare the FPGA mappings on the three different technologies.

IMPLEMENTATION RESULTS

Synthesis results for 8-point DCT and IDCT units are included in Table (1). These results indicate that the Xilinx FPGA implementations of DCT/IDCT can process higher numbers of frames per time unit, compared to the other two FPGA technologies. One reason for this considerable data processing speed is the utilization of coarse-grain reconfigurable resources available in the Virtex II FPGA. In particular, the usage of hard wired multipliers and fast carry chains lead to a severe acceleration of the implemented computations.

Table (1). Synthesis results for different FBGA technologies

<table>
<thead>
<tr>
<th>Implemented function</th>
<th>DCT</th>
<th>IDCT</th>
<th>DCT</th>
<th>IDCT</th>
<th>DCT</th>
<th>IDCT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Lucent ORCA-3C/3T series FPGA</td>
<td>Altera Aecx-1K series FPGA</td>
<td>Xilinx Virtex-II series FPGA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max Clock frequency (MHz)</td>
<td>22</td>
<td>22</td>
<td>16</td>
<td>16</td>
<td>54</td>
<td>60</td>
</tr>
<tr>
<td>No. of multipliers used</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>No. of LUTs used</td>
<td>1320</td>
<td>1488</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>No. of LCs used</td>
<td></td>
<td></td>
<td>1303</td>
<td>1482</td>
<td></td>
<td></td>
</tr>
<tr>
<td>No. of CLBs used</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>205</td>
<td>214</td>
</tr>
<tr>
<td>No. of SIF frames per second</td>
<td>896</td>
<td>877</td>
<td>647</td>
<td>647</td>
<td>2193</td>
<td>2469</td>
</tr>
<tr>
<td>No. of CCIR-TV frames per second</td>
<td>1219</td>
<td>214</td>
<td>158</td>
<td>158</td>
<td>536</td>
<td>600</td>
</tr>
<tr>
<td>No. of HDTV frames per second</td>
<td>40</td>
<td>40</td>
<td>29</td>
<td>29</td>
<td>100</td>
<td>112</td>
</tr>
</tbody>
</table>

It was particularly interested whether the FPGA implementations of the designs would be fast enough to meet the real time requirements of the selected video formats. For SIF and CCIR-TV, the requirements for real time processing rates are 25 frames per second. It can be observed in Fig. (6) that Xilinx FPGA implementations process the highest number of SIF frames per second. The other two FPGA technologies, using finer-grain resources, although slower, are capable of processing SIF frames at speeds, much higher than the required real-time rates (25 frames per second). Therefore, in this case the advantages of the Virtex II technology can not be utilized efficiently.
Fig. (6). Comparing different FPGA technologies to SIF Frames processing per second

Regarding CCIR-TV format, performance results impose similar conclusions see Fig. (7). All FPGA technologies provide DCT/IDCT processing speeds well above the required real time values.

Fig. (7). Comparing different FPGA technologies to CCIR-TV frames processed per second

The advantages of using coarse-grain reconfigurable resources for speeding up the DCT and IDCT operations are illustrated in Fig. (8). Only Xilinx FPGA is able to process twice the rate required by HDTV, which is 50 frames per second. The other two FPGA can not achieve the requirements for real time processing.

Fig. (8). Comparing different FPGA technologies to HDTV frames processed per second
SUMMARY AND CONCLUSIONS

It is reported in this paper the results from an investigation on reconfigurable implementations of DCT/IDCT mapped on different FPGA technologies. Synthesis and simulation results from the experiments indicate that real-time requirements of SIF, CCIR-ITV and even HDTV can be met by the implemented DCT and IDCT designs. From the reported results can conclude that all investigated FPGA implementations can speed up DCT based compression standards dramatically. However, for computationally intensive algorithms like DCT/IDCT better results can be achieved by coarser-grained reconfigurable logic, like the one realized by the Virtex II technology of Xilinx. It is intended in future, to integrate the investigated DCT/IDCT designs into a custom computing machine organization, called MOLEN [Vassiliadis 2001]. The MOLEN processors utilize microcode to control both reconfiguration and execution process of the reconfigurable unit. The primary goal will be to investigate the influence of FPGA reconfiguration time on the overall performance of the system.

REFERENCES


