Eng. & Tech. Journal, Vol.28, No. 10,2010

Power Control of Series-Parallel Resonant Inverter For Induction Heating Using Buck Converter

Dr. Turki K. Hassan* & Enaam A. Ali*

Received on: 17/5/2009
Accepted on: 16/2/2010

Abstract

The purpose of this work is to study, analyze, and design a half-bridge series-parallel resonant inverter for induction heating applications. A pulse width modulation (PWM)-based double integral sliding mode voltage controlled buck converter is proposed for control the induction heating power. This type of controller is used in order to obtain very small steady state error, stable and fast dynamic response, and robustness against variations in the line voltage and converter parameters. A small induction heating coil is designed and constructed. A carbon steel (C45) cylindrical billet is used as a load. The induction heating load parameters (R_L and L_L) are measured at the resonant frequency of 85 kHz. The parameters of the resonant circuit are chosen for operation at resonant. The inverter is operated at unity power factor by phased locked loop (PLL) control irrespective of load variations, with maximum current gain, and practically no voltage spikes in the switching devices at turn-off, therefore no snubber circuit is used for operation at unity power factor. A power MOSFET transistor is used as a switching device for buck converter and the IGBT transistor is used as a switching device for the inverter. A complete designed system is simulated using Matlab/Simulink. All the electronic control circuits are designed and implemented. The practical results are compared with simulation results to verify the proposed induction heating system. A close agreement between simulation and practical results is noticed and a good performance is achieved.

السيطره على قدره مبدل توالي- توازي التسخين الحثي باستخدام المحول نوع باك

الخلاصة

الغرض من البحث هو دراسة، وتحليل، وتصميم مبدل نصف- قنطري نوع توالي- توازي لتطبيقات التسخين بالحث. تم إقتراح وتصميم وتحليل مسيطر فولتية محول الفولتية المستمرة الى مستمرة نوع محول پاك والمضمن بطريقة عرض النبضة (PWM) وباستخدام المسيطر الأنزلاقي والتكاملي المزدوج للسيطرة على قدرة الحث بالتسخين. إن القدرة تتغير وفقا لتغير فولتية المبدل وهي تمثل ناتج فولتية محول پاك. تم إقتراح وإستخدام التكامل المزدوج للمتغير المسيطر عليه وإضافته الى سطح الأنزلاق للمسيطر الأنزلاقي وذلك لتقليل حالة الخطأ المستقرة للمحول، وإستجابته السريعة، ومقاومته العالية للاختلافات الحاصلة بين فولتية الخطأ ومعاملات المحول. تم تصميم الحمل من ملف صغير

أسطواني يلف حول أسطوانة معدنية من مادة (Carbon steel C45)،وتم قياس معاملات الحمل التي هي ال (R_L and L_L) عمليا عند تردد الرنين المختار 85 كيلو هيرتز. المبدل يعمل بعامل قدرة واحد باستخدام دائرة سيطرة نوع دائرة الطور المغلق (PLL) بغض النظر عن تغير الحمل أثناء التسخين, مع ربح تيارعالي, وكذلك في حالة الاطفاءلا توجد فولتية ناتئة لذلك لانحتاج الى ربط دائرة (snubber) اضافية .تم أستخدام ترنزستور ذات قدرة عالية نوع (MOSFET) كمفتاح لدائرة محول پاك، وترنزستور آخر ذات قدرة عالية نوع (IGBT) كمفتاح في دائرة المبدل. صمم النظام نظريا بإستخدام نظام المحاكاة (Matlab/Simulink)، وكل دوائر السسيطرة الألكترونية صممت وبنيت نظريا ومختبريا، النظام ككل بني عمليا. النتائج العملية تم مقارنتها مع النتائج النظرية لنظام الحث الحراري المقترح. حيث لوحظ تقارب هذه النتائج كما أثبتت هذه النتائج الاداء الجيد للنظام المقترح.

I. Introduction

Recently with the progress of power semiconductor devices, voltage or current source inverters have been researched and developed for induction heating applications such as melting and surface quenching. Resonant inverters type using power devices such as MOSFET and IGBT transistors offer reduced switching losses by soft-switching technique, therefore capable of operation at high frequency. A resonant inverter has no ability to control the output power by itself, therefore the following power control schemes have been proposed with a diode rectifier bridge as a DC power supply:

- Frequency control [1].
- Pulse width modulation [2].
- Phase shift control [3].
- Pulse density modulation control [4].
- Duty control [5].

These power control schemes, however, may result in an increase of switching losses and electromagnetic noises, because it is impossible for switching devices to be always turned on and off at zero current. In this paper, the output power of the inverter has to be controlled by adjusting the DC input voltage using a PWM-based double integral sliding mode voltage controlled buck converter as a variable DC power supply [5]. A phase locked loop (PLL) control circuit is used to maintain the operation of the inverter at unity power factor with maximum current ratio irrespective of load variations. Operation at unity power factor achieves ZCS (zero current switching) in a wide range of output power, thus resulting in a great reduction of switching losses and electromagnetic noises. Full analysis of half-bridge series-parallel resonant inverter and PWM-based double integral sliding voltage controlled buck converter are presented in section II and III respectively. The design, simulation and experimental setup of complete system are explained in section IV. In section V the simulation

and experimental results are obtained and compared to validate the proposed power controlled induction heating system.

II. Series-Parallel Resonant Inverters

A simplified circuit diagram of a half-bridge series-parallel resonant inverter is shown in Fig. (1-a). A module of dual (IGBT) transistor is used. The induction heating load is modeled by a series combination of its equivalent resistance R_L and inductance L_L.

In Fig. (1-b), typical on-off timings of the transistors and diodes at a leading power factor are shown. For a steady state cycle of the inverter operation, there are basically four distinct intervals. The harmonic analysis approach can be employed to develop expressions for the output circuit variables [6].

The analysis implies the following simplifications and assumptions:

(a) The input voltage of the inverter is constant. (b) The IGBT's and diodes are ideal.

(c) The parallel and series capacitors (C_P and C_S) are treated as ideal capacitances with no losses.

The instantaneous inverter output voltage can be expressed in Fourier series as:

$$V_o(t) = \frac{2V_i}{\pi}\sum_n^{\infty}\frac{1}{n}\sin(n\omega t) \ldots (1)$$

Where n is odd, V_i is the input voltage of the inverter and ω is the angular frequency.

The nth harmonic impedance of the series and parallel circuits can be expressed as:

$$Z_{Sn} = R_S + j\left(n\omega L_S - \frac{1}{n\omega C_S}\right) \ldots (2)$$

$$Z_{Pn} = \frac{R_L + jn\omega L_L}{1 - n^2\omega^2 L_L C_P + jn\omega R_L C_P} \quad \ldots\ldots (3)$$

$$I_{1n} = \frac{V_{on}}{Z_{1n}} \quad \ldots\ldots (4)$$

Where

$$V_{on} = \frac{2V_i}{n\pi} \text{ and } Z_{1n} = Z_{Sn} + Z_{Pn} \ldots (5)$$

The time-domain expression for the output current can be represented by:

$$i_1(t) = \sum_{n=1}^{\infty} I_{1n}\sin(n\omega t - \phi_{1n}) \ldots (6)$$

$$I_{1n} = |\bar{I}_{1n}| \text{ and } \phi_{1n} = \tan^{-1}(Z_{1n}) \ldots (7)$$

The induction heating coil voltage V_2 (t) and current $i_2(t)$ can be evaluated as:

$$V_{2(t)} = \sum_{n=1}^{\infty} V_{2n}\sin(n\omega t + \theta_n) \ldots (8)$$

Where

$$V_{2n} = I_{1n}|Z_{Pn}| \text{ and}$$
$$\theta_n = \tan^{-1}(Z_{Pn}) - \phi_{1n} \quad \ldots (9)$$

For the coil current,

$$i_2(t) = \sum_{n=1}^{\infty} I_{2n} \sin(n\omega t + \emptyset_{2n}). \quad (10)$$

Where

$$I_{2n} = \frac{V_{2n}}{\sqrt{R_L^2 + (n\omega L_L)^2}} \quad \text{and}$$

$$\emptyset_{2n} = \theta_n - \tan^{-1}\left(\frac{n\omega L_L}{R_L}\right) \ldots\ldots. (11)$$

The RMS values of the inverter output current, and induction heating coil current and voltage can be calculated as

$$I_1 = \left(\sum_{n=1}^{\infty} \frac{I_{2n}^2}{2}\right)^{\frac{1}{2}}, \; I_2 = \left(\sum_{n=1}^{\infty} \frac{I_{2n}^2}{2}\right)^{\frac{1}{2}},$$

and

$$V_2 = \left(\sum_{n=1}^{\infty} \frac{V_{2n}^2}{2}\right)^{\frac{1}{2}} \quad \ldots\ldots. (12)$$

Considering only the fundamental component for simplicity, the magnitude of the current gain can be written in the form

$$\frac{I_2}{I_1} = \left[(1 - \omega^2 L_L C_P)^2 + (\omega C_P R_L)^2\right]^{\frac{-1}{2}}$$

…… (13)

The maximum operating frequency

$$f_m = \frac{1}{2\pi}\sqrt{\frac{1}{L_L C_P} - \frac{R_L^2}{2L_L^2}} \quad \ldots\ldots\ldots (14)$$

And its corresponding value is

$$\left(\frac{I_2}{I_1}\right)_{max} = \left[\frac{C_P R_L^2}{L_L}\left(1 - \frac{C_P R_L^2}{4L_L}\right)\right]^{-\frac{1}{2}} \ldots. (15)$$

For our practical cases,

$$\frac{C_P R_L^2}{L_L} \ll 1 \quad \ldots\ldots\ldots (16)$$

Then, equation (13) reduces to

$$\left(\frac{I_2}{I_1}\right)_{max} \approx \frac{1}{R_L}\sqrt{\frac{L_L}{C_P}} \quad \ldots\ldots\ldots\ldots (17)$$

It is a simple matter to show that the inverter runs at unity power factor with maximum current gain, i.e., operation at point *B* as illustrated in Fig. (2), if the series compensating capacitance C_S takes approximately the following value:

$$C_S \approx \frac{C_P}{\frac{L_S}{L_L} - 0.5} \quad \ldots (18)$$

The frequency at point B is chosen according to the induction heating application.

The overall inverter circuit efficiency can be expressed as:

$$\eta = \frac{I_2^2 R_L}{I_1^2 R_S + I_2^2 R_L}\eta_C = \frac{\eta_C}{\frac{1}{\left(\frac{I_2}{I_1}\right)^2}\frac{R_S}{R_L} + 1} \ldots (19)$$

Where

$$\eta_C \approx R_w / R_L \quad \ldots\ldots\ldots (20)$$

η_C is the heating coil efficiency and R_w denotes the work-piece reflected resistance. Maximum overall inverter circuit efficiency occurs at maximum current gain

$$\eta_{max} \approx \frac{1}{\frac{1}{\left(\frac{I_2}{I_1}\right)^2_{max}}\frac{R_S}{R_L} + 1}\frac{R_w}{R_L} \ldots\ldots. (21)$$

III. Sliding Mode Controllers

The basic principle of SM control is to design a certain sliding surface in its control law that will direct the trajectory of the state variables toward a desired origin. In the case of a single switch DC–DC converter, it is appropriate to have a control law that adopts a switching function such as

$$u = \frac{1}{2}(1 + sign(S)) \quad \text{…. (22)}$$

Where u is the logic state of the converter's power switch, and S is the instantaneous state variable's trajectory which, in the case of a second-order controller is described as:

$$S = \alpha_1 x_1 + \alpha_2 x_2 + \alpha_3 x_3 \quad \text{….. (23)}$$

α_1, α_2, and α_3 represent the control parameters, usually referred to as sliding coefficients, and x_1, x_2, and x_3 denote the desired state feedback variables to be controlled. By enforcing S = 0, a sliding surface (plane), as shown in Fig. (3) can be obtained.

In brief, the entire SM-control process can be divided into two phases. In the first phase (reaching phase), regardless of the starting position, the controller will perform a control decision that will drive the trajectory of the state variables to converge to the sliding surface as shown in Fig. (3-a). This is possible through the compliance of the so-called hitting condition.

When the trajectory is within a small vicinity of the sliding surface, it is said to be in SM operation, which is the second phase of the control process. The controller will give a series of control actions via switching such that the trajectory is maintained within a small vicinity of the sliding surface and is concurrently directed toward the desired reference at origin O Fig. (3-b) [7] ,[8],[9],[10] ,[11].

Hence, when the system enters into SM operation, its equivalent trajectory can be ideally described as S = 0. This also defines the dynamic characteristic of the system, which can be designed by the proper choice of control parameters, i.e., sliding coefficients.

For double integral sliding mode (DISM) voltage controlled buck converter, the controlled state variables are the voltage error x_1, the voltage error dynamics (or the rate of change of voltage error) x_2 , the integral of voltage error x_3, and the double integral of the voltage error x_4, which are expressed as [8]

$$\begin{cases} x_1 = V_{ref} - \beta v_o \\ x_2 = \dot{x}_1 \\ x_3 = \int x_1 dt \\ x_4 = \int (\int x_1 dt) dt \end{cases} \quad \text{…… (24)}$$

Substitution of the buck converter's behavioral models under continuous conduction mode (CCM) of operation into the time differentiation of (24) gives the dynamical model of the proposed system as:

$$\begin{cases} \dot{x}_1 = \frac{d(V_{ref}-\beta v_o)}{dt} = -\frac{\beta}{C} i_C \\ \dot{x}_2 = \frac{\beta}{r_L C^2} i_C - \frac{\beta v_i}{LC} u + \frac{\beta v_o}{LC} \\ \dot{x}_3 = x_1 = V_{ref} - \beta v_o \\ \dot{x}_4 = \int x_1 dt = \int (V_{ref} - \beta v_o) dt \end{cases} \quad \text{.....(25)}$$

The equivalent control signal of the proposed DISM voltage controller is obtained by solving:

$$\left(\frac{dS}{dt}\right) = \alpha_1 \dot{x}_1 + \alpha_2 \dot{x}_2 + \alpha_3 \dot{x}_3 + \alpha_4 \dot{x}_4 = 0 \text{.(26)}$$

This gives:

$$u_{eq} = \left.\begin{aligned} &\frac{\beta L}{\beta v_i}\left(\frac{1}{r_L C} - \frac{\alpha_1}{\alpha_2}\right) i_C + \frac{\beta v_o}{\beta v_i} + \frac{\alpha_1}{\alpha_2}\frac{LC}{\beta v_i}\left(V_{ref} - \beta v_o\right) \\ &+ \frac{\alpha_4}{\alpha_2}\frac{LC}{\beta v_i}\int (V_{ref} - \beta v_o) dt \end{aligned}\right\} \text{.(27))}$$

Where C, L and r_L denote the capacitance, inductance, and instantaneous load resistance respectively; $V_{ref,}$ V_i and V_o denote the reference, instantaneous input, and instantaneous output voltages respectively; β denotes the feedback network ratio; i_L, i_C, and i_r denote the instantaneous inductor, instantaneous capacitor, and instantaneous output currents respectively; and u_{eq} is the equivalent control signal which is continuous and bounded by 0 and 1, i.e., $0 < u_{eq} < 1$.

In PWM form, the proposed DISM voltage controller for the buck converter inherits the expression [8]:

$$V_c = -K_1 i_C + K_2 (V_{ref} - \beta V_o) + K_3 \int (V_{ref} - \beta V_o) dt + \beta V_o$$

..... (28)

Where

$$\begin{cases} K_1 = \beta L \left(\frac{\alpha_1}{\alpha_2} - \frac{1}{r_L C}\right) \\ K_2 = \frac{\alpha_3}{\alpha_2} LC \\ K_3 = \frac{\alpha_4}{\alpha_2} LC \end{cases} \quad \text{..... (29)}$$

K_1, K_2, K_3, are the fixed gain parameters in the proposed controller.

Fig. (4) shows a schematic diagram of the derived PWM-based DISM voltage controller for the buck converters [8].

IV. System Simulation and Implementation

This section covers the design, simulation, and implementation of the half-bridge series-parallel resonant inverter for induction heating. A block diagram for the system is shown in Fig. (5). A phased locked loop is used to maintain the operation of the inverter at unity power factor in order to maximize the input power and reduce the switching losses of power devices. A three phase bridge full wave rectifier is used as a DC power supply and a capacitor is connected across the terminals of the rectifier as a smoothing filter. A PWM-based double integral sliding mode voltage controlled buck converter is used to obtain adjustable DC supply voltage to the inverter. Two equal capacitors (CS_1, CS_2) and resisters (RS1, RS2) are connected as shown in Fig. (5) across the output of buck converter terminals for the junction N to be at midpotential

with half the buck converter output voltages across each capacitor and resistor. These equal voltages are applied to the half bridge series-parallel resonant inverter circuit. The power of the inverter can be varied when the output voltage of buck converter is varied.

A. System Design

A laboratory scale induction-heating coil is designed and constructed to obtain proper match between heating circuit and the power source. The heating coil is a 7-turn of axial length 10 cm and external diameter 6.5cm. It is making from 1 cm diameter round

Copper tubing. The work-piece is a 15cm long, a carbon steel-C45 cylindrical billet diameter of 5cm.The induction heating coil parameters R_L and L_L depend on the inverter operating frequency and their experimental values at 85 KHz are respectively 0.278Ω, 1.6μH.

The value of the parallel capacitor (C_P) is calculated according to the equation (14)

$$C_p \approx 2.1 * 10^{-6}\ F \quad \text{..... (30)}$$

A value of the series capacitor (C_S) is chosen as (0.6 μF) in order to run the inverter at unity power factor with maximum current gain. Current gain is calculated according to equation (17),

$$\left(\frac{I_2}{I_1}\right)_{max.} \approx (3.2) \quad \text{..... (31)}$$

A series resistance R_S and series inductance L_S are experimentally found to be 0.25Ω and 4.86μH respectively. The resistance of the induction heating coil at no load (R_c) is experimentally found to be 0.012Ω.

The work-piece reflected resistance (R_w) can be calculated as

$$R_w = R_L - R_c = 0.278 - 0.012 = 0.266\Omega \quad \text{... (32)}$$

The maximum efficiency of the inverter circuit can be calculated according to the equation (21) as

$$\eta_{max} \approx \frac{1}{\frac{1}{\left(\frac{I_2}{I_1}\right)^2_{max}}\frac{R_S}{R_L}+1}\frac{R_w}{R_L} = 86.9 \quad \text{...(33)}$$

The insulated gate bipolar transistor (IGBT) is selected for the construction of the inverter. The type of the used IGBTs is 2MBI150N-060. Two equal capacitors (C_{S1}, C_{S2}) of (7000μF, 75VDC) value for each, and two equal resisters of 560Ω, 5 watt value for each are used to obtain a midpotential point N as shown in Fig. (5). A step-down DC-DC buck converter illustrated in Fig. (5), consists of a semiconductor switching device (power MOSFET type IRF540N), a shottky diode (D) type (SB360), used as a freewheeling diode, filter inductor (L), filter capacitor (C), and a small resistor of 0.1Ω, 25watt value is connected in series with the filter capacitance (C) as a current sensor. This current signal is fed to (DISM) controller circuit. The input voltage to the buck converter is applied from the rectifier bridge circuit and the
output voltage of the converter is applied to the inverter circuit.

The minimum value of filter inductance ($L_{(min.)}$) is expressed as [12]

$$L_{(min.)} = \frac{(1-D)R_L}{2f} \quad \text{……. (34)}$$

For typical values of D (duty ratio) = 0.5, and f =25KHZ, R_L=5Ω, the boundary (L (min.) = 50μH). For (L > L (min.)), the converter operates in the continuous conduction mode (CCM). A value of (100μH) is chosen, the filter inductor current i_L in the (CCM) consists of a dc component I_o with a superimposed triangular ac component flows through the filter capacitor as a current I_c, this current causes a small voltage ripple across the dc output voltage V_o. To limit the peak-to-peak value of the ripple voltage below a certain value (V_r), the filter capacitor C must be greater than $C_{(min.)}$ [12]

$$C_{(min.)} = \frac{(1-D)V_o}{8V_r L f^2} \quad \text{…….. (35)}$$

At D=0.5, $(V_r/V_o) = 1\%$, L=62μH, and f=25KHZ, the minimum capacitance is equal to (200μF). A value of (250μF) is chosen.

The proposed PWM-based double integral sliding mode voltage controller for buck converter is designed by finding the parameters of equation (28). The controller is designed to give a critically response with a bandwidth (f_{BW}) of 2.5 kHz value, the sliding coefficients are: [8]

$$\frac{\alpha_1}{\alpha_2} = 4\pi f_{BW} = 4\pi(2.5*10^3) = 31400 \quad \text{..(36)}$$

$$\frac{\alpha_3}{\alpha_2} = 4\pi^2 f_{BW}^2 = 4\pi^2(2.5*10^3)^2 = 246490000 \quad \text{…(37)}$$

The reference voltage is set as V_{ref} =2.5V, which gives

$$\beta = \frac{V_{ref}}{V_{o(max)}} = 0.0416 \quad \text{…..... (38)}$$

Where $V_{o(max)}$ the maximum value of buck converter is applied voltage which is equal to 60V. The Parameters K_1 and K_2 are calculated using equations (29) which are,

$$K_1 = 0.1306 \quad \text{……. (39)}$$

$$K_2 = 6.168 \quad \text{…….. (40)}$$

K_3 is chosen equal to (2000) according to the required damping response. According to the above values, the implemented control signal (V_c) equation is,

$$V_c = \left.\begin{aligned} &-0.1306 i_c + 0.0416 v_o + 6.168(V_{ref} - \beta v_o) \\ &+2000 \int (V_{ref} - \beta v_o)\, dt \end{aligned}\right\} \quad \text{..(41)}$$

B. System Simulation

The complete system shown in Fig. (5) is simulated using Matlab/Simulink. The equations that are derived for half-bridge series-parallel resonant inverter circuit in section two and the equations for the PWM-based DISM voltage controlled buck converter that are presented in section three are used in the simulation.

A Simulink circuit for the system is implemented, and Fig. (6) shows this circuit. The designed parameters are used in the simulink circuit.

c. System Implementation

The complete designed system shown in Fig. (5) is experimentally constructed. The phase locked-loop (PLL) circuit, IGBT gate drive circuit, and PWM-based DISM voltage controller circuit are designed and built. In this section, all electronic circuits are presented and described.

1. Phase Locked-Loop(PLL) Control Circuit

The parameters of the induction heating load vary during the heating cycle. It thus becomes necessary to change the operating frequency of the inverter in order to maintain its power factor near unity. The phased locked-loop (PLL) control circuit as seen from Fig. (7), plays a major role in the inverter operation. The

Former has the task of keeping a zero cross-current switching mode, irrespective of load variations.

This achieved by using a high frequency current transformer with ratio of 20/1 and a resistance of 10Ω 5watt value is connected across the secondary of this transformer to produce a voltage proportional to the inverter current (i_1). This signal is applied to the comparator IC type (C272) to convert it to a square wave. The output of the comparator then applied to PLL IC type (TC4046BC) pin1 ($S1_{in}$ Signal). A two control pulses, the first control pulses is applied to gate drive circuit from pin4 of the PLL IC (VCO_{out}), and the other control pulses is produced using NAND gate type (TC4011BF) as shown in Fig. (7).

When the frequencies of ($S1_{in}$ and $S2_{in}$) signals are unequal, phase detector gives an output signal S_{out} indicating frequency difference, and when locked it indicates a phase difference. The signal S_{out} is used to shift the VCO toward lock before capture then holds the frequencies in lock. Locked condition is obtained when both ($S1_{in}$ and $S2_{in}$) signals have equal frequencies with their phase difference equal to zero.

2. Gate drive circuit

Recently, the insulated gate bipolar transistor is gaining popularity for its relatively high speed and low gate power requirements. Its control terminals are the gate and emitter. The device turns on when a voltage greater than its gate emitter threshold voltage is applied between the gate and emitter, Fig. (8) shows the IGBTs drive circuit developed for the work.

The turn-on and turn-off pulses from the PLL control circuit output terminals (A and B) are first amplified to appropriate magnitude, and then sent through small pulse transformer to drive the MOSFET's (K2645). The upper and lower pairs of MOSFET's form push-pull drivers for gating IGBTl and IGBT2, respectively. The pulse transformers with ferrite cores isolate the IGBT's from the control circuitry. The coupling capacitors (0.22 µF) prevent any amount of dc current from flowing in the primary windings and saturating the transformers. Back-to-back connected zener diodes (RD4A) limit the MOSFET gate to source voltage to about four Volts, and

protect the gates of the MOSFET's against over voltages induced by drain voltage spikes on the gates. Rapid turn-off times for the IGBT achieved with the speed-up capacitors (0.1μ*F*). The (10Ω) resistors, in series with the MOSFET's, provide supply protection against short circuits in case the MOSFET's conduct at the same time.

3. PWM-Based DISM Voltage Controlled Buck Converter

The analog circuit using operation amplifiers, PWM integrated circuit, and optocoupler and power MOSFET driver is implemented shown in Fig. (9), the gains of operational amplifiers are chosen according to equation (44). A reference of 2.5V value type (TL431) is used to obtain a reference set value with high accuracy. Two resistors R_1 and R_2 are used as a voltage divider to produce the feedback output voltage which is equal to βV_o where β is equal to

$$\frac{R_2}{R_1+R_2} \qquad \ldots\ldots. (42)$$

A small resistor of 0.1Ω 25watt is used to measure the current of the filter capacitor (C) and applied to (DISM) controller. The operational amplifiers type (LM318) is used. The control signal (V_C) which represents the output of last stage of operational amplifiers as shown in Fig. (9) is applied to the PWM IC type (SG3526) which its output is a PWM control pulses. A PWM control signal is isolated using optocoupler type (6N137), and then applied to a driver type (ULN2003) in order to produce very small rise and fall times for control pulses. A switching frequency is chosen as a 25 KHz by a proper values of resistor and capacitor connected to the (9, 10) of PWM IC (SG3526).

V. Results and Discussion

A matlab Simulink and the experimental circuits that are used to obtain the simulation and experimental results, set up respectively.

Fig. (10) shows the experimental waveforms of the inverter current (i_1) at switching frequency of (75 kHz, 85kHz, 100kHz) and DC applied voltage of 20V, the amplitudes of the experimental currents are equal to (7 A, 4 A, 4A) respectively.

Fig. (11) shows the simulated waveforms of the inverter current (i_1) at switching frequency of (75 kHz, 85kHz, 100kHz) and DC applied voltage of 20V, the amplitudes of the simulated currents are equal to (6.5 A, 4 A, 4.5A) respectively. A close agreement between simulated and experimental waveforms is noticed.

Fig. (12) shows the experimental waveforms of the load current (i_2) at switching frequency of (75 kHz, 85kHz, 100kHz) and DC applied voltage of 20V, the amplitudes of the experimental currents are equal to (12A, 10A, 8A) .

Fig. (13) shows the simulated waveforms of the load current (i_2) at switching frequency of (75 kHz,

85kHz, 100kHz) and DC applied voltage of 20V, the amplitudes of the experimental currents are equal to (12.5A, 10A, 9A). A close agreement between simulated and experimental waveforms is noticed.

Fig. (14) shows the experimental waveforms of the inverter current (i_1) at switching frequency of (75kHz, 85kHz,100 kHz) and DC applied voltage of 40V, the amplitudes of the experimental currents are equal to (12 A, 8 A, 11.8A) respectively.

Fig. (15) shows the simulated waveforms of the inverter current (i_1) at switching frequency of (75kHz, 85kHz, 100 kHz) and DC applied voltage of 40V, the amplitudes of the experimental current is equal to (12 A, 8 A, 12.5A) respectively. A close agreement between simulated and experimental waveforms is noticed.

Fig. (16) shows the experimental waveforms of the load current (i_2) at switching frequency of (75kHz, 85kHz, 100 kHz) and DC applied voltage of 40V, the amplitudes of the experimental currents is equal to (22A, 18A, 15A) .

Fig. (17) shows the simulated waveforms of the load current (i_2) at switching frequency of (75kHz, 85kHz, 100kHz) and DC applied voltage of 40V, the amplitudes of the experimental currents are equal to (28A, 21A, 19A).

In the Figures (10) to (17), a good agreement between simulation and experimental results is noticed for low values of inverter current (i_1) and load current (i_2) especially when the inverter applied dc voltage equals to 20V. But when the applied voltage is increased to 40V, the currents i_1 and i_2 are increased and a small difference between simulation and experimental results is noticed. This difference is due to variation of the induction heating load parameters at higher currents, this is not taken into account for simulation, also the capacitors are considered as a pure (Zero equivalent series resistance (ESR)) for simulation which is not practically satisfied.

Fig. (18) shows the simulated and experimental curves of the ratio of inverter current (i_1) to the load current (i_2) (i_2/i_1) against switching frequency at 20V applied voltage. The ratio has a maximum value of 2.6 at resonant frequency 85 kHz.

Fig. (19-a) shows the experimental waveforms of (IGBT) collector to emitter voltage at 75 KHz and at 40V DC applied voltage; there is no voltage spike in this waveform when the inverter operates around the resonant frequency, and therefore no snubber circuit is needed.

Fig. (19-b) shows the experimental waveforms of (IGBT) collector to emitter voltage at 85 KHz and at 40V DC applied voltage; there is no voltage spike when the inverter operates at resonant frequency.

Table (1) shows the input power against the DC applied voltage of the inverter for switching frequencies 75 kHz, 85 kHz, and 100 kHz respectively. In this table the power is increased when the DC voltage is increased, for the same applied voltage the power is the

highest at resonance frequency of 85 KHz value.

Table (2) shows the temperature variation of induction heating load (a billet of a carbon steel C45) against time at input power of 290 watt, 85 KHz switching frequency and 60V dc applied voltage.

A simulation and experimental results are provided to validate the theoretical design of a double integral sliding mode voltage controlled buck converter.

Fig. (20) shows the simulated and experimental waveforms of the output voltage of buck converter. The input voltage to the buck converter equals to 60V. The switching frequency equals to 25 KHz. The output voltage of the buck converter equals to 20V. A close agreement between simulated and experimental waveforms is noticed.

Fig. (21) shows the simulated and experimental waveforms of the output voltage of buck converter of buck converter that are equal to 40V. The applied voltage equal to 60V and the switching frequency equals to 25 KHz. A close agreement between simulated and experimental waveforms is noticed.

Fig. (22-a) shows the experimental waveforms of the gate-source voltage of the power MOSFET. For the applied voltage to the converter equals to 60V, and the output voltage of the converter equals to 40V.

Fig. (22-b) is the same of Fig. (22-a) but with buck converter output voltage of 20V.

The series-parallel resonant inverter is a nonlinear load to the buck converter, therefore the stability and steady state error must be tested for different values of dc output voltage .The ability of the double integral sliding mode voltage controller which is used to obtain small steady state error and stable response also must be tested. Simulation and experimental results for the DC output voltage of buck converter show very small steady state error, stable response and good performance of the suggested sliding mode controller for different values of dc output voltage.

VI. Conclusions

All electronic circuits are designed and built. The induction heating system is tested practically. Based on simulation and experimental results, the following aspects can be concluded:

1-The output power of the induction heater is controlled by varying the applied DC voltage of the inverter which represents the output of buck converter.

2- Maximum current gain (i_2/i_1) is obtained when the inverter is operated at resonance frequency with unity power factor.

3- There is no voltage spike in the switching devices at turn-off when the inverter is operated at resonance frequency or around this frequency.

4- Approximately sinusoidal waveforms for the inverter current i_1 and load current i_2 are obtained when the switching frequency equals to resonance frequency at unity power factor.

5- The inverter operates at unity power factor irrespective to the induction heating load parameters variation due to the operation of the phase locked loop circuit.

6- In this work, the maximum temperature of the billet that is obtained equals to 120 C°. Some practical limitations to increase the temperature of billet above 120 C° are found. These limitations are:

a- A good electrical insulator is needed between the billet and the coil suitable for high temperature. The used insulator is not sufficient.

b- A good thermal insulation is needed to localize the heat through the billet (decreasing the heat radiation). In this work, no thermal insulator is used.

c- Suitable high frequency high KVAR capacitors with low equivalent series resistance (ESR) are required. In this work, a bank of capacitors connected in parallel is used, these capacitors has low KVAR and high ESR.

When the above requirements are met, the power can be increased and higher temperature will obtained since the rating of switching devices can satisfy a power of approximately 2 KW value.

References

[1]-A. Dmowski, R. Bugyi, and P.Szewczyk, "A Novel Series-Resonant DC-DC Convverter with Full Control of Output Voltage at no Load Conditions. Compute Simulation Based Design Aspects," IEEE/ IAS Annu. Meet. 1992, PP. 924-928.

[2]-M. Nakaoka, Y. J. Kim, H. Ogiwara, and H. Vemura, "Modern Digital Controlled Constant High Frequency PWM Resonant DC-DC Converter Using Lumped Parasitic Reactive Circuit Components of High Voltage Transformer and Feeding Cable New Practical Application," IEEE/ IAS Annu. Meet. 1991, PP. 1088-1097.

[3]-L. Grajales, J. A. Sabate, K. R. Wang, W. A. Tabisz,and F. C. Lee, " Design A 10 KW, 500 kHz Phase-Shift Controlled Series-Resonant Inverter for Induction Heating," IEEE/ IAS Annu. Meet. 1993, PP. 843-849.

[4]-H. Fujita H. Akagi, "Pulse-Density-Modulated Power Control of a 4KW, 450KHz Voltage-Source Inverter for Induction Melting Applications", IEEE Trans. on Indust. Application Vol. 32, No. 2, March/April 1996.

[5]-Name-Ju Park, Dong-Yan Lee and Dong-Seok Hyun, "A Power Control Scheme with Constant

Switching Frequency in Class D Inverter for Induction Heating Jar Application" , IEEE Trans. On Indust. Electronics, Vol. 54, No. 3, June 2007.

[6]-Mokhtar Kamil, Shigehino Yamamoto, and Minoru Abe, "A 50-150 KHz Half-Bridge Inverter for Induction Heating Applications", IEEE Trans. On Indust. Elect. Vol. 43, No. 1, February 1996.

[7]-Siew-Chong Tan,Y. M. Lai and Chi K. Tse., "General Design Issues of Sliding-Mode Controller for DC-DC Converters", IEEE Trans. on Indst. Electro. Vol. 55, No. 3, March 2008.

[8]-Siew-Chong Tan,Y.M.Lai and Chi K. Tse., "Indirect Sliding Mode Control of Power Converter Via Double Integral Sliding Surface",IEEE Trans. On Power Electron.,Vol. 23,No.2, March 2008.

[9]-Fossas, L. Martínez, and J. Ordinas, "Sliding mode control reduces audio susceptibility and load perturbation in the Cuke converter", IEEE Trans. Circuits Syst. I, vol. 39, no. 10, pp. 847–849, Oct. 1992.

[10]-Siew-Chong Tan, "A Fixed-Frequency PWM Based Quasi-Sliding-Mode Controller for Buck Converters", IEEE Trans. on power Electron, Vol. 20, No. 6, November 2005.

[11]-S. C. Tan, Y. M. Lai, and C. K. Tse, "A unified approach to the design of PWM based sliding mode voltage controller for basic DC-DC converters in continuous conduction mode", IEEE Trans. Circuits Syst. I, vol. 53, no. 8, pp. 1816–1827, Aug. 2006.

[12]-Muhammad H. Rashid, Power Electronics Hand Book, 2006.

Appendix

Photos of the experimental system:

-Fig. (A1) Full bridge rectifier and inverter circuits.

-Fig. (A2) From left phase-locked loop circuit and gate drive circuit.

-Fig. (A3) power circuit of (DISM) controlled buck converter.

-Fig. (A4) induction heating load with temperature gauge.

-Fig. (A5) control circuit of (DISM) controlled buck converter.

Table (1)

Input power against DC applied voltage, at (75 kHz),(85kHz), and (100kHz)

DC Applied Voltage	Input Power at (75 kHz)	Input Power at (85 kHz)	Input Power at (100 kHz)
20V	30W	35W	20W
30V	50W	55W	50W
40V	105W	110W	100W
45V	120W	160W	150W
50V	160W	195W	160W
60V	200W	290W	220W

Table (2)

Load temperature against time for switching frequency (85 KHz), DC Voltage (60 V), Input Power (290W)

Time (min.)	Temperature (C^o)
0	15^o
0.5	30^o
1	60^o
1.5	70^o
2	80^o
2.5	90^o
3.5	110^o
4	120^o

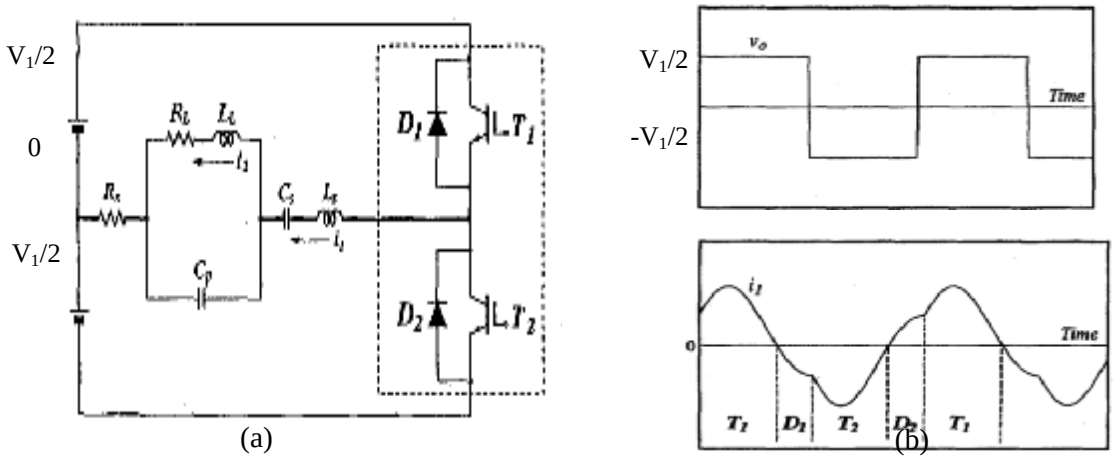


Figure (1): (a) Simplified Circuit of the Series-Parallel Resonant Inverters.
(b) Typical steady state waveforms of the inverter output current i_1 and inverter output voltage V_o at a leading power factor [6].

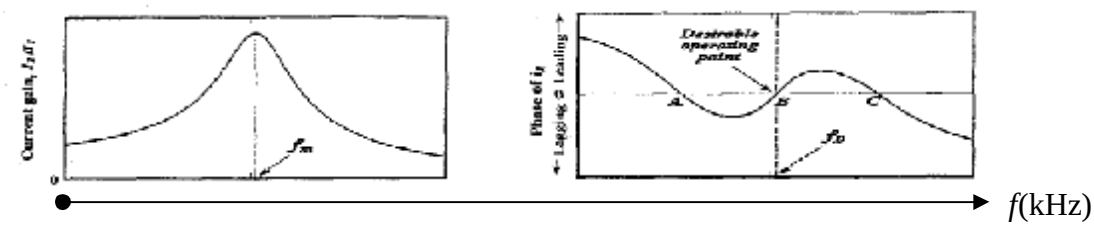


Figure (2) The inverter runs at unity power factor with maximum current gain, operation at point B [6].

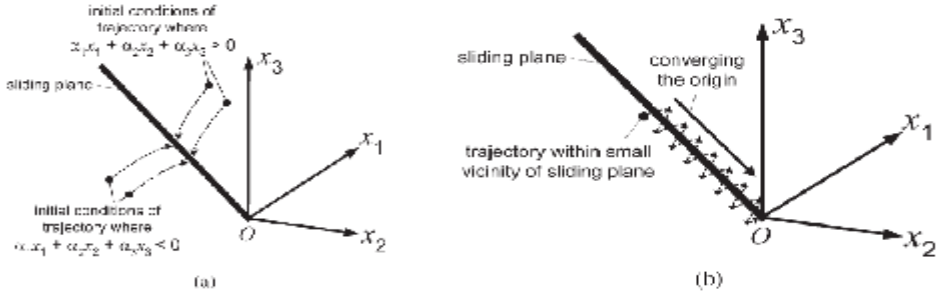


Figure (3): Graphical representations of state variables' trajectory behavior in SM control process. (a) Phase 1—illustrating trajectory converging the sliding plane irrespective of its initial condition. (b) Phase 2 illustrating trajectory being maintained within small vicinity from the sliding plane and concurrently being directed to converge to the origin O [10].

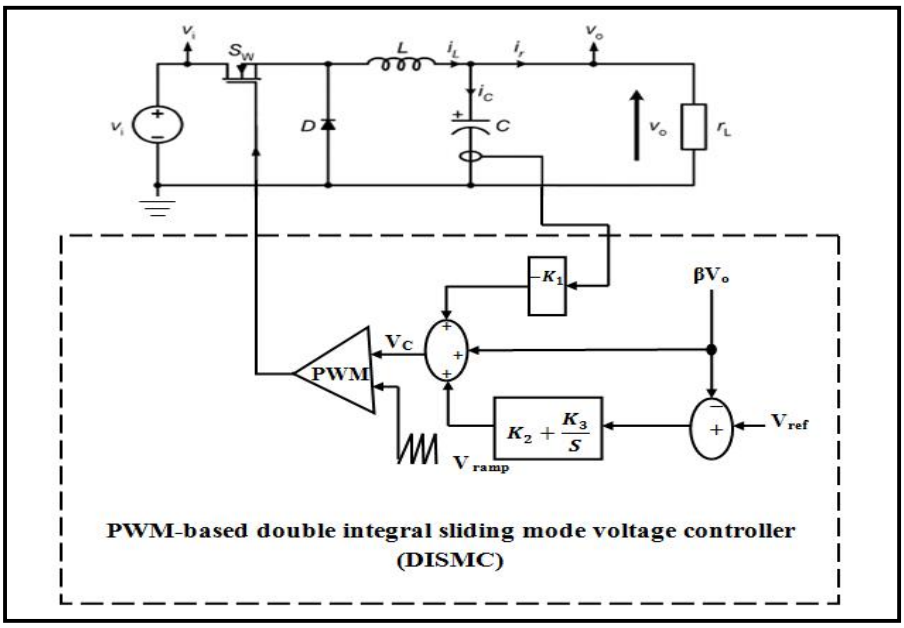


Figure (4) Proposed pulse width modulation based SM voltage controller for buck converters .

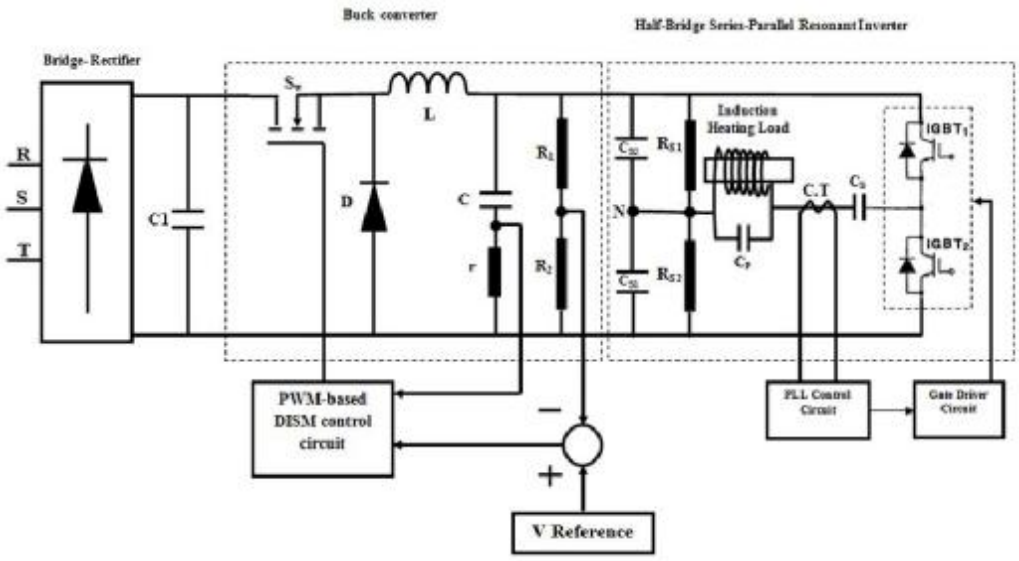


Figure (5) Proposed System Configurations

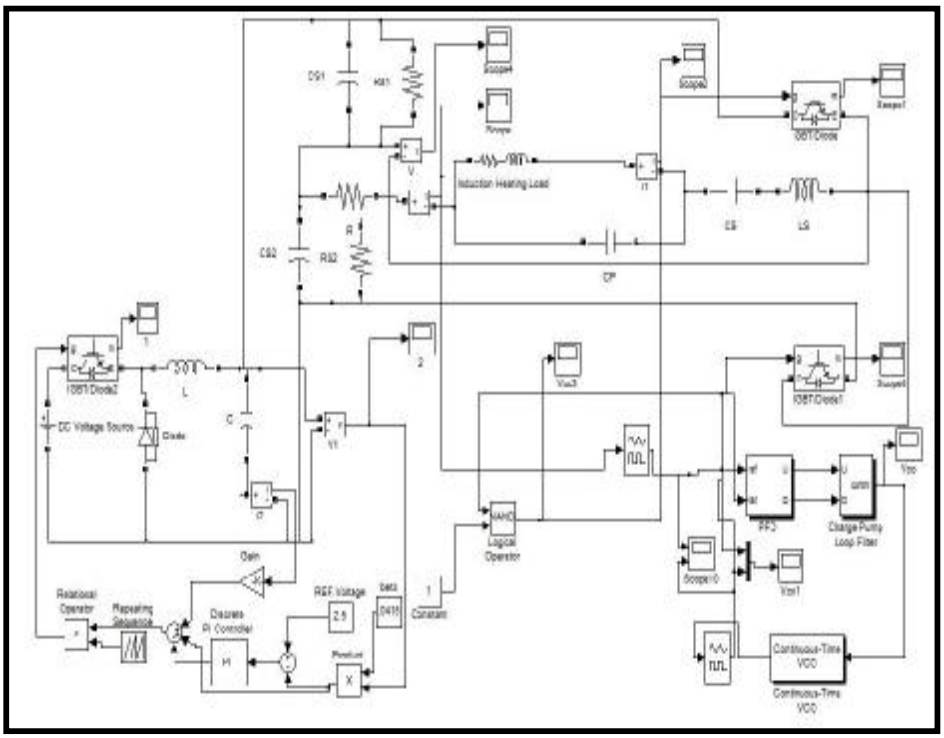


Figure (6): The Simulink for the Proposed System.

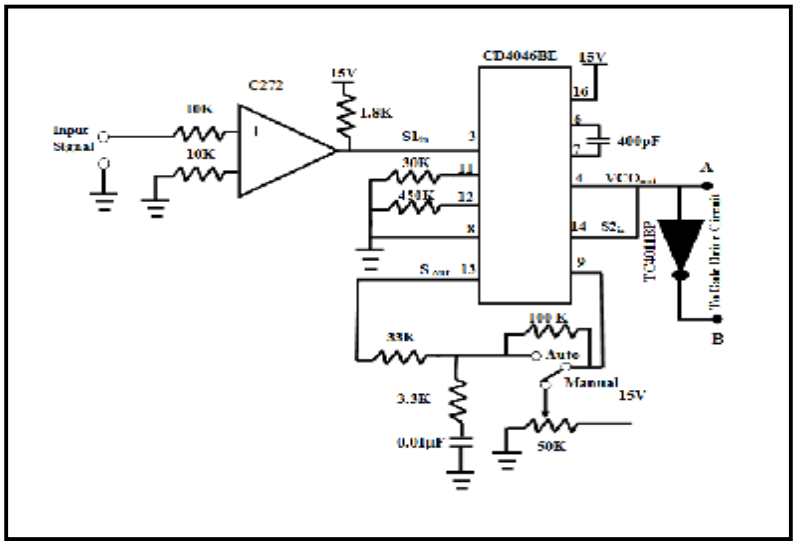


Figure (7): Phase-locked loop circuit.

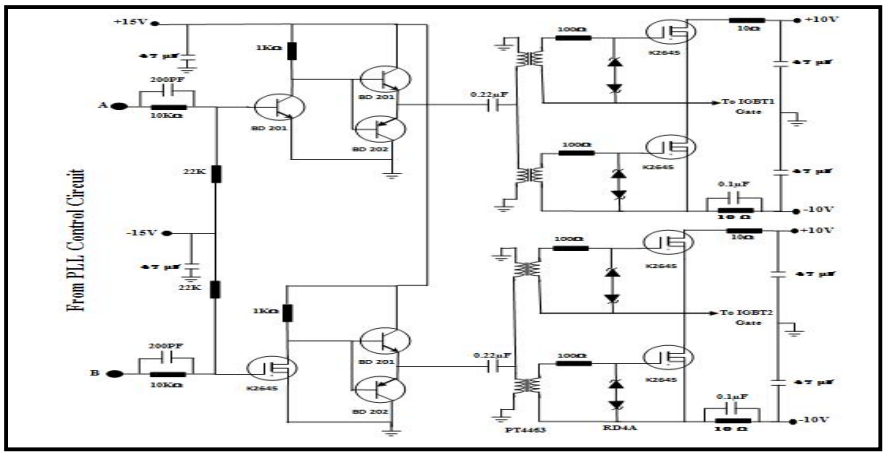


Figure (8) IGBT Gate Drive Circuit

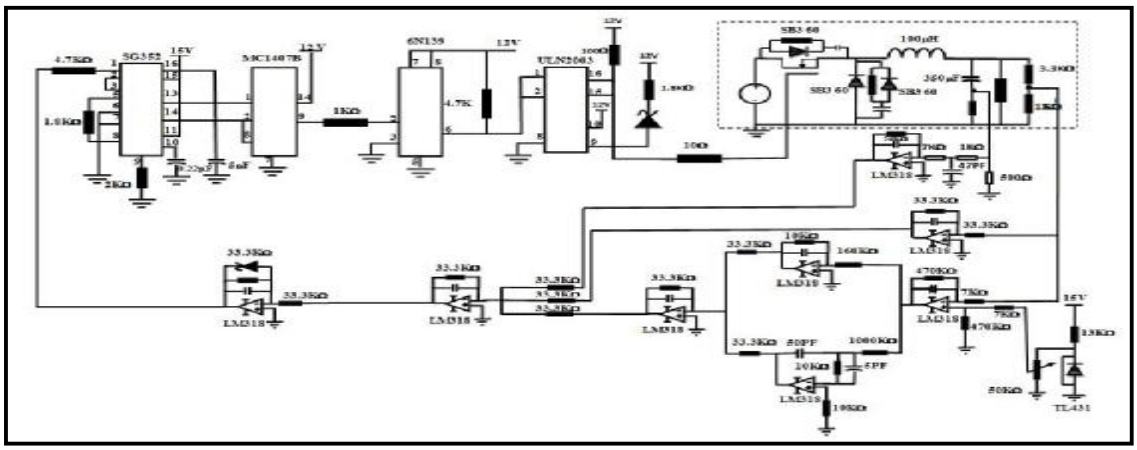
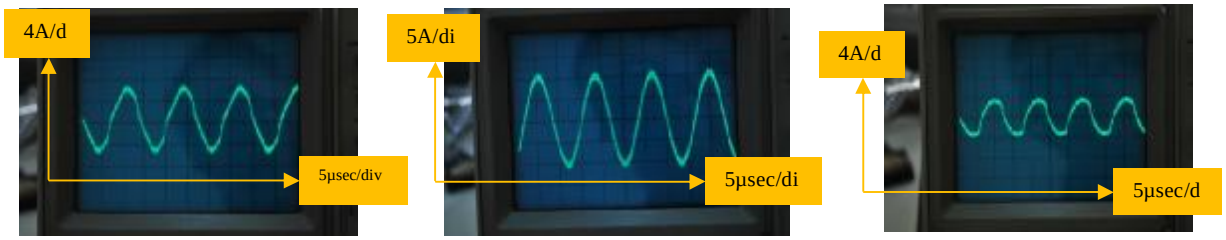
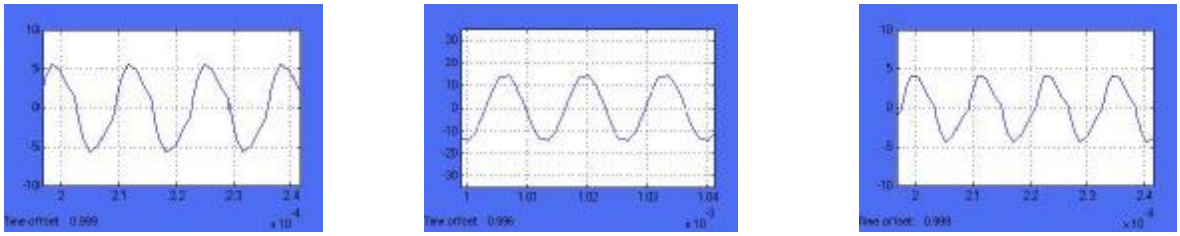


Figure (9) Full Schematic Diagram of the PWM-Based DISM voltage controlled bucks Converter



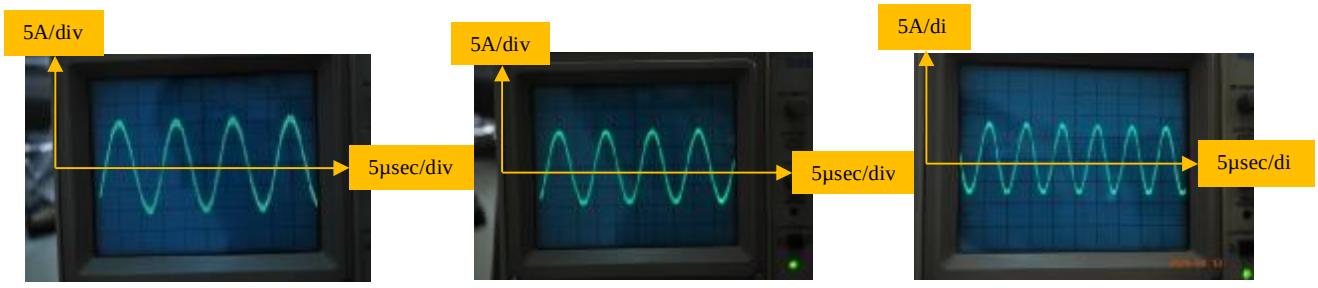
(a) (b) (c)

Figure (10) Experimental waveforms of inverter current (i1) at operating frequency (a) (75 KHz), (b) (85 kHz), and (c) (100 kHz) at 20V DC input voltage.



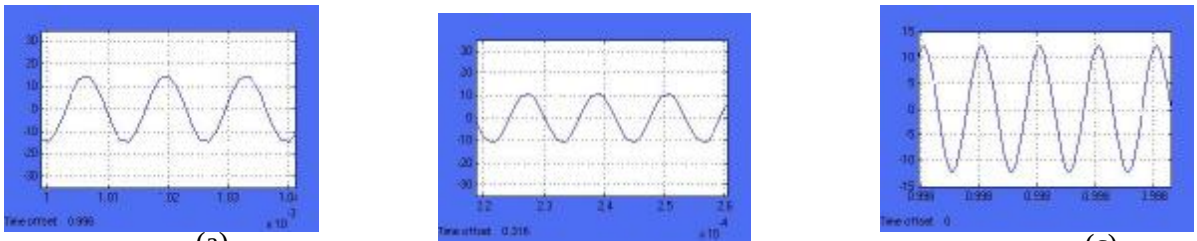
(a) (b) (c)

Figure (11): Simulated waveforms of inverter current (i1) at operating frequency (a) (75 KHz), (b) (85 kHz), (c) (100 kHz) at 20V DC input voltage.



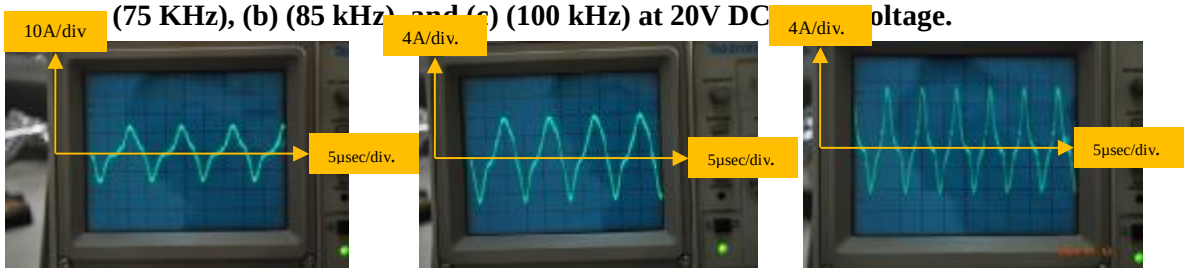
(a) (b) (c)

Figure (12): Experimental waveforms of load current (i2) at operating frequency (a) (75 KHz), (b) (85 kHz), and (c) (100 kHz) at 20V DC input voltage.



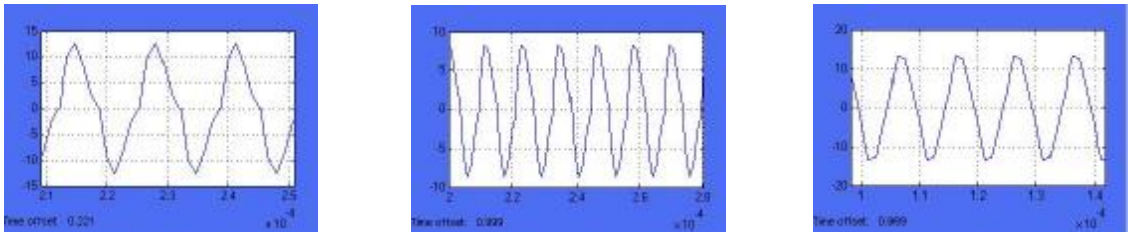
(a) (b) (c)

Figure (13): Simulated waveforms of load current (i2) at operating frequency (a) (75 KHz), (b) (85 kHz), and (c) (100 kHz) at 20V DC input voltage.



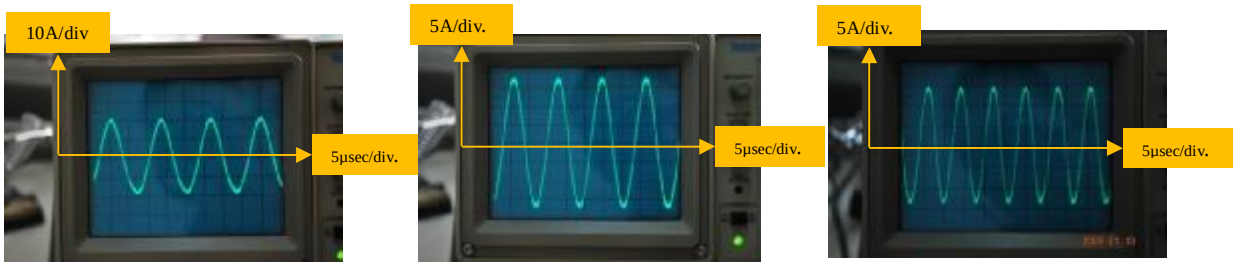
(a) (b) (c)

Figure (14): Experimental waveforms of inverter current (i1) at operating frequency (a) (75 KHz), (b) (85 kHz), and (c) (100 kHz) at 40V DC input voltage.



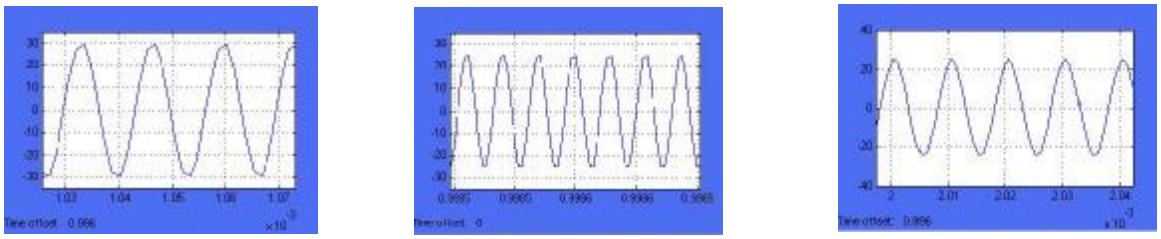
(a) (b) (c)

Figure (15) Simulated waveforms of inverter current (i1) at operating frequency (a) (75 KHz), (b) (85 kHz), and (c) (100 kHz) at 40V DC input voltage.



(a) (b) (c)

Figure (16) Experimental waveforms of load current (i2) at operating frequency (a) (75 KHz), (b) (85 kHz), and (c) (100 kHz) at 40V DC input voltage.



(a) (b) (c)

Figure (17) Simulated waveforms of load current (i2) at operating frequency (a) (75 KHz), (b) (85 kHz), and (c) (100 kHz) at 40V DC input voltage.

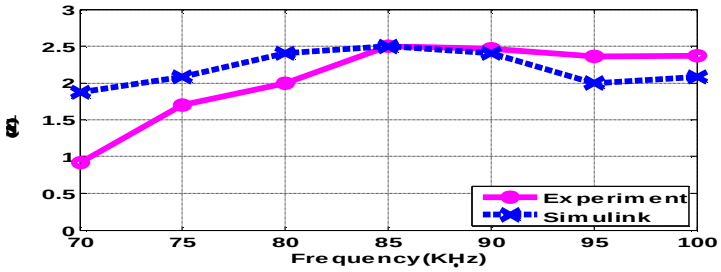


Figure (18) A plot of the experimental and simulated curves of the ratio (i2/i1) against switching frequency at 20V DC input voltage

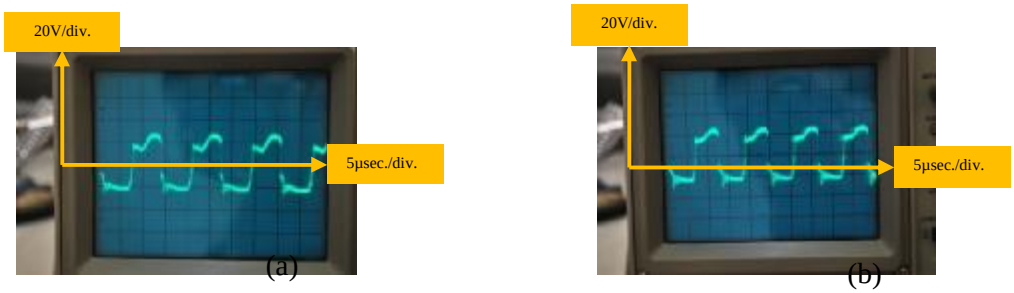


Figure (19) Waveform of the (IGBT) collector-emitter voltage at: (a) (75 kHz) and (b) at (85 kHz) at 40V DC applied voltage.

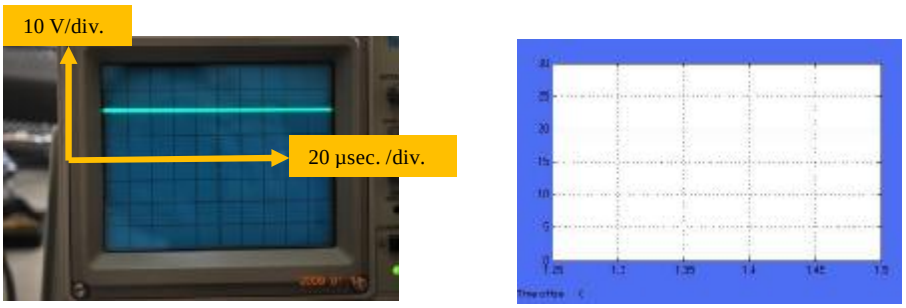
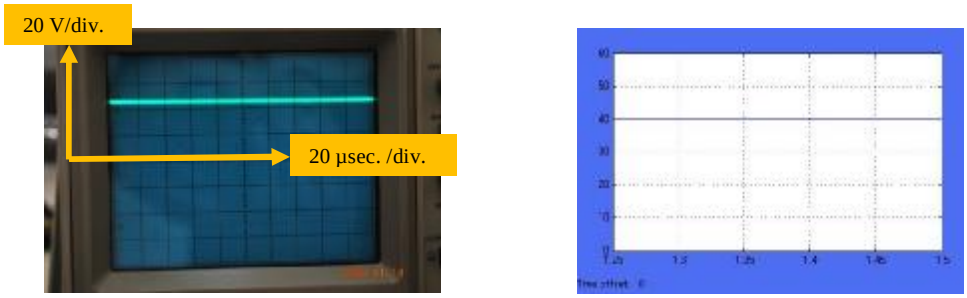
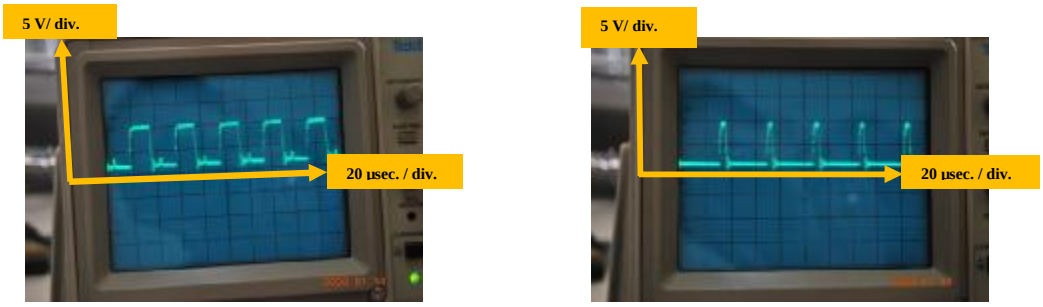


Figure (20): (a) Experimental and (b) Simulated waveforms of 20V output voltage of buck converter at switching frequency (25 KHz) and 60V DC input voltage.



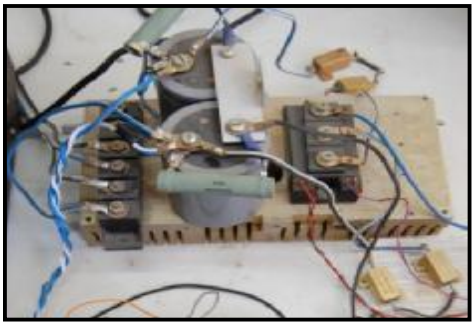
(a) (b)

Figure (21): (a) Experimental and (b) Simulated waveforms of 40Voutput voltage of buck converter at switching frequency (25 KHz) and 60V DC input voltage.

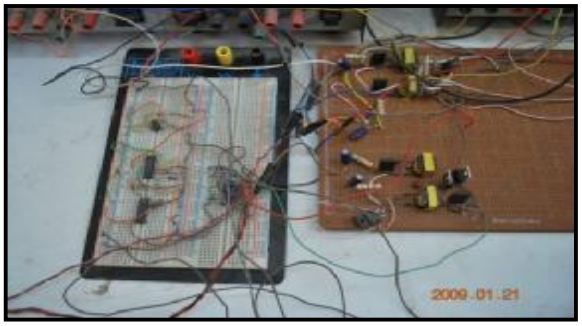


(a) (b)

Figure (22): Waveform of the (MOSFET) gate source voltage at (25 KHz) and at: (a) 40V output voltage of buck converter, (b) 20V output voltage of buck converter.



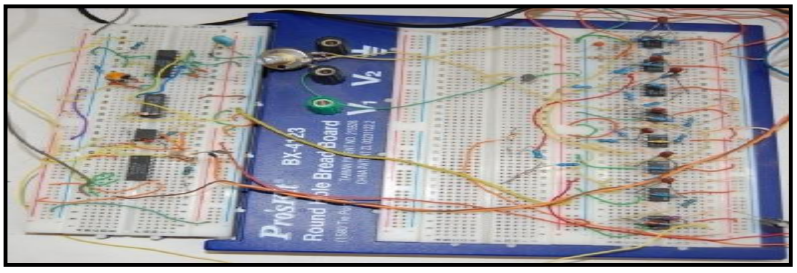
(A1)



(A2)

(A3)

(A4)



(A5)