Design and Implementation of MC-CDMA Technique Using FPGA

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ABSTRACT

Multicarrier Code Division Multiple Access (MC-CDMA) is attractive technique for high speed wireless data transmission; it's a combination of Orthogonal Frequency Division Multiplexing (OFDM) and Code Division Multiple Access (CDMA). OFDM employs a number of orthogonal subcarriers, this increases the symbol duration while the CDMA technique provides high capacity over other conventional multiple access schemes. In this paper discusses implementation of base band MC-CDMA system using the FPGA technique, all modules are designed using VHDL programming language. The electronic functional performance of designed circuits is tested by simulations using VHDL programming language on XILINX ISE 9.2i. The proposed model is designed using (Fast Fourier Transform/ Inverse Fast Fourier Transform) and the spreading code used is the gold code, the implementation of the proposed model using Spartan-3A/3AN, XC3S700N-3FGG484 FPGA of Xilinx family.

Keywords: MC-CDMA, OFDM, CDMA, FPGA.

تنفيذ تقنيات تعدد النواقل-تعدد الوصول بتقسيم الترميز باستخدام مصفوفة البوابات المنطقية المبرمجة

الخلاصة

تعتبر تقنية تعدد النواقل-تعدد الوصول بتقسيم الترميز تقنية متميزة لأرسال البيانات لاسلكيا بسرع عالية,هي عبارة عن مزيج من تقنية مزج تقسيمات التردد المتعامدة وتقسيم الرمز المتعدد الوصول. تقنية مزج تقسيمات التردد المتعامدة تستخدم عدد من النواقل المتعامدة وهذا سوف يزيد من مدة الرمز, بينما تقنية تقسيم الرمز المتعدد الوصول تزود سعة عالية عن بقية أنظمة الوصول المتعدد التقليدية. في هذا البحث نناقش تنفيذ تقنيات تعدد النواقل-تعدد الوصول بتقسيم الترميز باستخدام مصفوفة البوابات المنطقية المبرمجة ,كل الوحدات تم تصميمها بأستخدام لغة البرمجة (VHDL) لقد تم فحص الاداء الالكتروني للدوائر المصممة بأستخدام فحص المحاكاة الذي يزوده برنامج XILINX ISE 9.2i الموديل المقترح تم تصميمه بأستخدام تحويل فورير السريع وتحويل فورير السريع العكسي ورمز الانتشار المستخدم هو الرمز الذهبي أما تنفيذ التصميم المقترح تم بأستخدام البوابات المنطقية المبرمجة من نوع XC3S700N-3FGG484 Spartan-3A/3AN من عائلة Xilinx .

INTRODUCTION

MC-CDMA is formed by combining orthogonal frequency division multiplexing (OFDM) with code division multiple accesses (CDMA) . The OFDM is well suited for high data rate applications and the CDMA is a multiplexing technique where number of users is simultaneously available to access a channel[1,2]**.** With MC-CDMA a data symbol is transmitted over N narrowband subcarriers with each subcarrier being encoded based on the spreading code. Different users transmit over the same set of subcarriers but with a spreading code which maintains the orthogonality. The resulting signal has an orthogonal code structure in the frequency domain. If the number of subcarriers and the spacing between them is appropriately chosen, it is unlikely that all of the subcarriers will be located in a deep fade and consequently frequency diversity is achieved[3].

OFDM is a special case of multi-carrier transmission, where a data stream is transmitted over a number of lower rates sub-carriers. On classical frequency division multiplexing the total band is divided into N non overlapping frequency channels, while on OFDM the band is divided into a number of overlapping frequency channels but with orthogonal frequencies, the consequence is a better use of the available spectrum [4]. The orthogonality is achieved by making the peak of each subcarrier signal coincide with the null of the other subcarrier signals resulting in a perfectly aligned and spaced subcarrier signal [5].

CDMA is a multiple-access scheme based on spread-spectrum communication techniques , it spreads the message signal to a relatively wide bandwidth by using a unique code that reduces interference, enhances system processing, and differentiates users. Spreading is obtained via a multiplication of the baseband data information by a spreading sequence of pseudorandom signs, sometimes called pseudonoise (PN) or code signal, before transmission [6,7] . FPGAs have achieved high levels of success in many signal processing systems, in particular in the area of digital communications. FPGA signal processing platforms can service the many complex tasks performed in a modern communication transmitter and receiver , it give optimal device utilization while conserving both board space and system power and offer greater device speed and greater device density [8,9].

SYSTEM DESCRIPTION

A random code sequence of zeros and ones is generated using the gold code to spread the incoming bit stream. For implemented model as shown in the Figure (1), modulation is carried out with BPSK signal constellation ,to achieve multi carrier modulation the OFDM block is used.

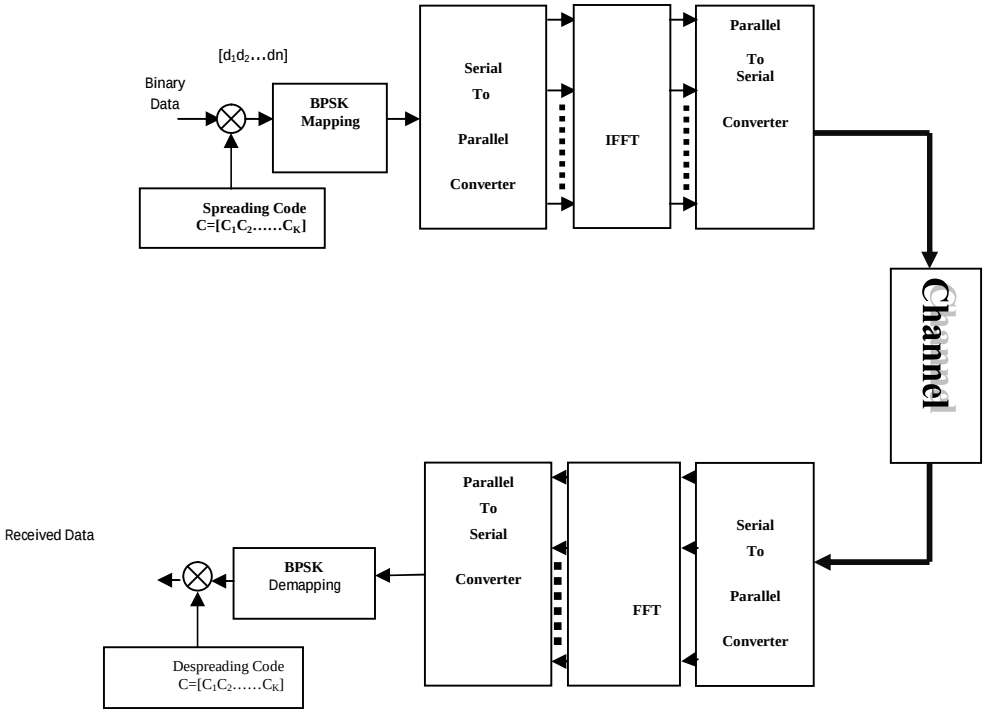

Figure (1) Proposed MC-CDMA system model.

Transmitter Design

At the transmitter side there is a number of blocks programmed and tested separately first then connected together to form the transmitter part, these blocks are:

1- Generation of spreading code part.
2- Spreading technique part.
3- The BPSK mapping part.
4- The serial to parallel conversion part.
5- The inverse fast Fourier transform part.
6- The parallel to serial conversion part.

Spreading code is done by using Gold code as a spreading code; Gold code are constructed from a modulo-2 addition of two PN code sequences ,after programmed the circuit and checked by the Xilinx9.2i program ,the RTL part of the circuit is shown in Figure (2) and the behavioral simulation of the circuit as shown in Figure (3).

Figure (2) RTL part of Gold code generation.

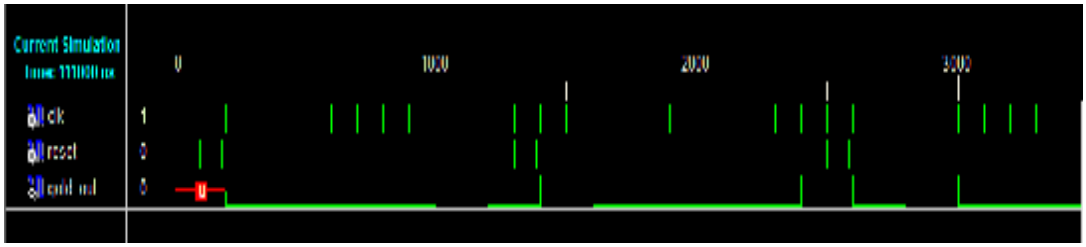

Figure (3) Behavioral simulation of Gold code.

BPSK modulator operates on a single bit at a time; the modulator takes a single bit as input and outputs 2-levels representing the real and imaginary as shown in Figure (4). The BPSK mapping, which is used here was purely real, a (1) is represented by the symbol (1 + j0) and a (0) was represented by (−1 + j0), the output is purely real and the modulator has an imaginary part of its output constantly assigned to (0) and representation of the output will be according to the 2's complement and the behavioral simulation of the circuit as shown in Figure (5).

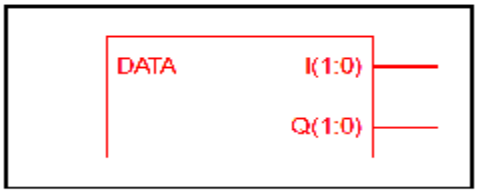

Figure (4) RTL circuit describe BPSK entity.

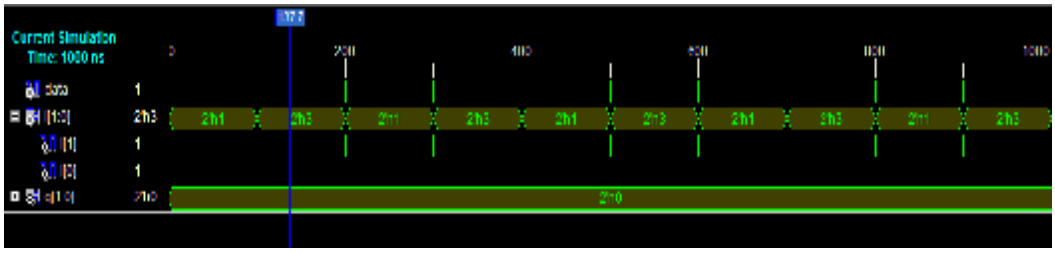

Figure (5) Behavioral simulation of BPSK modulation

In the programming of an IFFT operation, the butterfly method computation is used in which the input lines will pass through the equations of the algorithm of butterfly method as shown below :

X(0)=x(0) + x(4)+ x(2)+ x(6)+ x(1)+ x(5)+ x(3)+ x(7)
X(4)= x(0) + x(4) + x(2)+ x(6)- x(1) - x(5)- x(3)- x(7)
X(2)=x(0)+ x(4)- x(2)- x(6)+ jx(1)+ jx(5)- jx(3)- jx(7)
X(6)=x(0)+ x(4)- x(2)- x(6)- jx(1)- jx(5)+ jx(3)+ jx(7)
X(1)=x(0)-x(4)+ jx(2)- jx(6)+ 0.7071x(1)+ j0.7071x(1)
- 0.7071x(5)- j0.7071x(5)
- 0.7071x (3)- j0.7071x(3)
+ 0.7071x (7) + j0.7071x (7)
X(5)=x(0)- x(4)+ jx(2)- jx(6)- 0.7071x(1)- j0.7071x(1)
+ 0.7071x (5) + j0.7071x (5)
+ 0.7071x (3) + j0.7071x (3)
- 0.7071x (7)- j0.7071x(7)
X(3)=x(0)- x(4)- jx(2)- jx(6)- 0.7071x(1)+ j0.7071x(1)
+ 0.7071x (5) - j0.7071x (5)
+ 0.7071x (3) - j0.7071x (3)
- 0.7071x (7) + j0.7071x (7)
X(7)=x(0)- x(4)- jx(2)- jx(6)+ 0.7071x(1)- j0.7071x(1)
- 0.7071x (5) + j0.7071x (5)
- 0.7071x (3) + j0.7071x (3)
+ 0.7071x (7)- j0.7071x(7)

In order to program this set of equations it must be separated as real part and imaginary part and each equation will called as path so it must arranged again each one of input lines must be divided into two parts one real and other imaginary as shown below taken one path like path 5 it mean X (5) and other parts will be arranged in the same way:

Path (5)

X(5) = x(0) – x(4) +jx(2) - jx(6) - 0.7071 x(1) –j 0.7071x(1) + 0.7071x(5) + j 0.7071 x(5) +0.7071 x(3) + j 0.7071 x(3) - 0.7071 x(7) - j 0.7071 x(7)

X(5) = [x(0) + jx(0)] – [x(4) +j x(4)] + j [x(2) + j x(2)] - j [x(6) + j x(6)] - 0.7071 [x(1) + jx(1)] – j 0.7071[x(1) + jx(1)] + 0.7071 [x(5) + jx(5)] + 0.7071j [x(5) + jx(5)] + 0.7071 [x(3) + jx(3)] + j 0.7071 [x(3) + jx(3)] - 0.7071 [x(7)+ jx(7)] - j 0.7071 [x(7) + jx(7)]

X(5)real = [x(0)re – x(4)re - x(2)ima +x(6)ima] - 0.7071 [x(1)re + x(1)ima – x(5)re + x(5)ima – x(3)re + x(3)ima + x(7)re – x(7)ima]

X(5)ima = j [x(0)ima – x(4)ima + x(2)re - x(6)re] -j 0.7071 [x(1)ima + x(1)re – x(5)ima - x(5)re – x(3)ima – x(3)re - x(7)ima + x(7)ima]

After arranging all equations as in path(5) then they programmed and obtain an RTL part of the IFFT module as shown in Fig.(6) (here in the programming the output will be replace to be y instead of x in order to distinguish from the input name letter) and the behavioral simulation of the circuit as shown in Fig(7) .

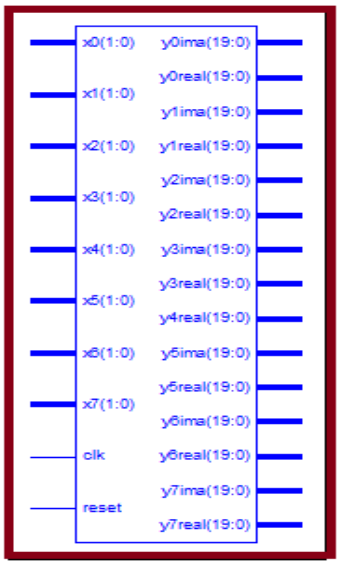

Figure (6) RTL circuit that describe IFFT entity.

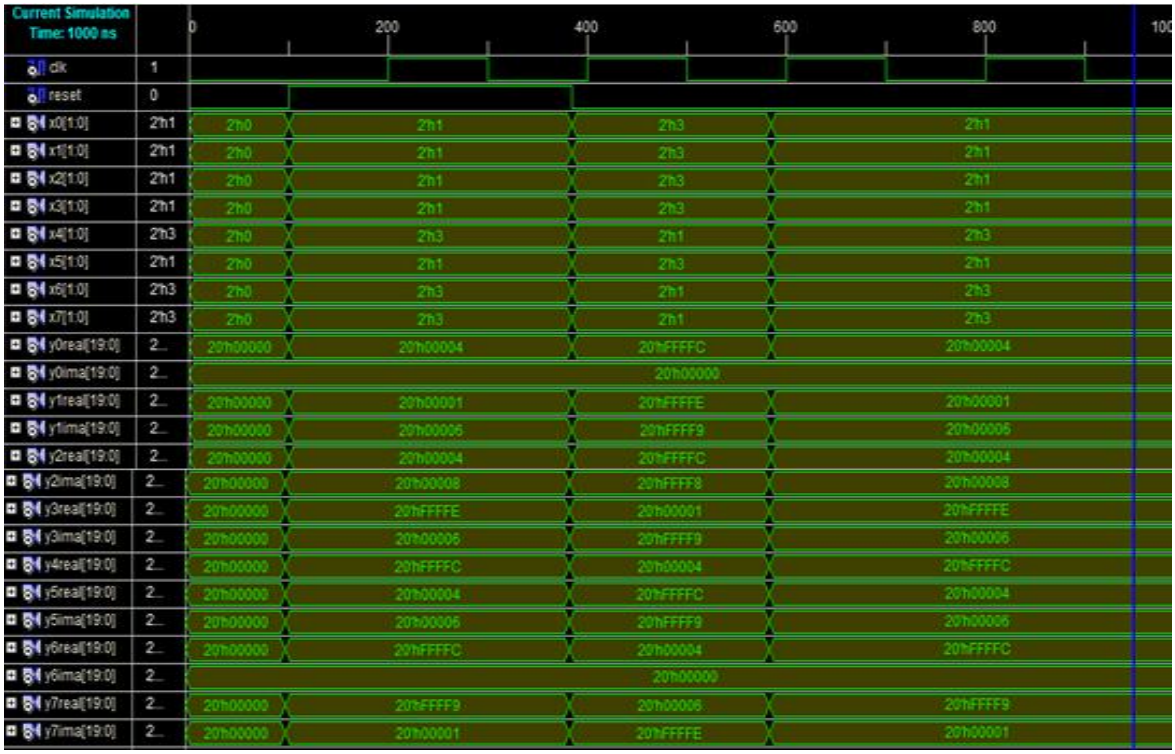

Figure (7) Behavioral simulation IFFT circuit.

RECEIVER DESIGN

At the Receiver side, also there is a number of blocks programmed and tested separately first, then connected together to form the receiver parts. These blocks are:

1- The serial to parallel conversion part.
2- The fast Fourier transform part.
3- The parallel to serial conversion part.
4- The BPSK demapping part.
5- Generation of despreading code part.
6- Despreading technique part.

Spreading code is designed with the same procedure of the transmitter part because it must be same , BPSK demodulator at the receiver will take the input from parallel to serial convertor, it will take either (+1) or (-1)as the inputs and output one bit either 0 or 1, the output of this part must be the same as the input that enter to the BPSK modulator transmitter side ,the circuit which describe the entity is as shown in Figure (8) and the behavioral simulation of the circuit is as shown in Figure (9).

Figure (8) RTL circuit describe BPSK demodulator

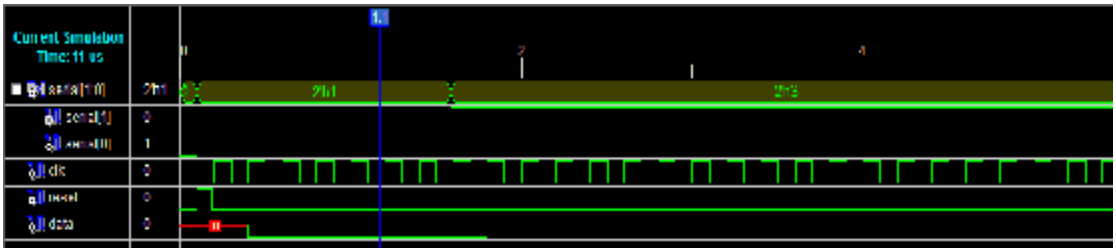

Figure (9) Behavioral simulation of the BPSK demodulator.

FFT block will programmed in the same way of programming the IFFT in the transmitter part and after programming the paths it will give the RTL part as shown in Figure (10) and the behavioral simulation of the circuit as shown in Figure (11).

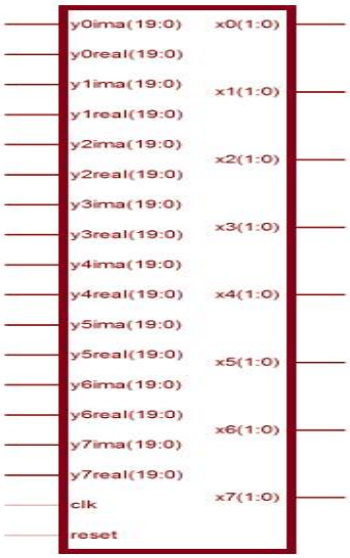

Figure (10) RTL circuit describe FFT entity.

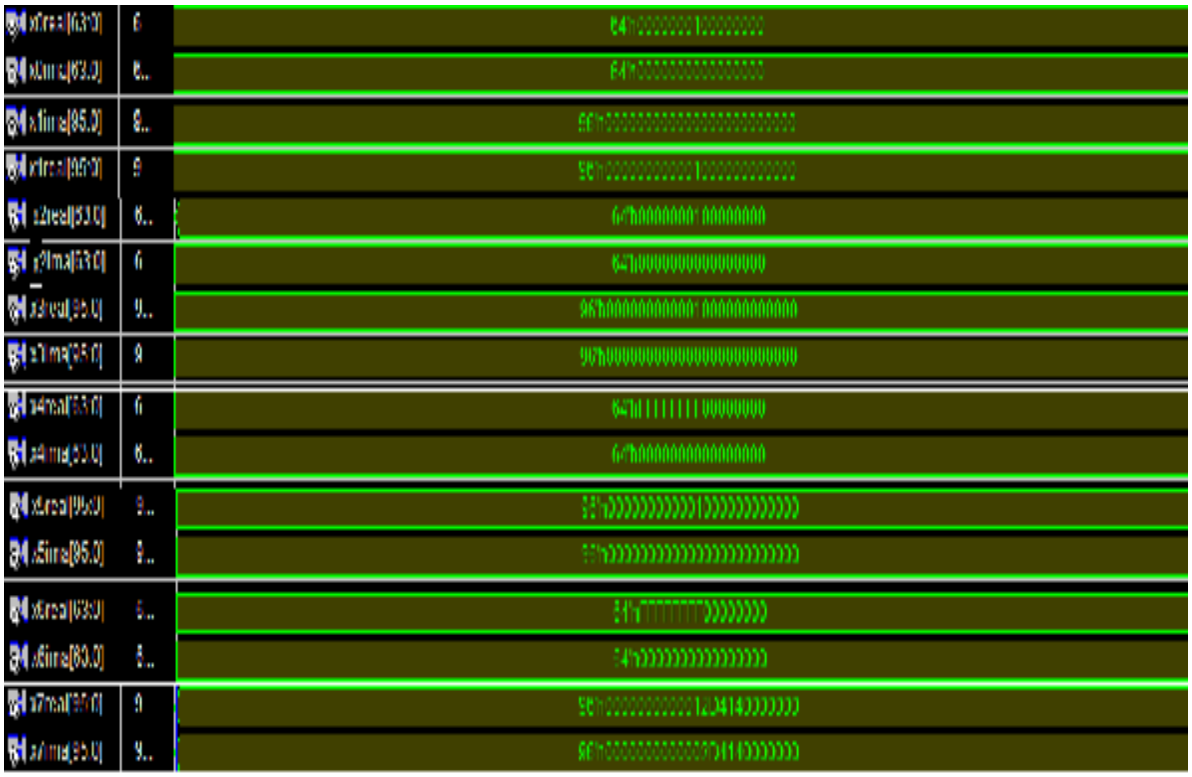

Figure (11) Behavioral simulation of the FFT circuit.

VHDL SIMULATION

Since all the parts of the transmitter and receiver were completed and tested separately ,now all parts were connected together to build the system then check the design summary to see if the utilization is it fitted with the size of the FPGA IC to complete and download it on the IC. After the circuit is synthesized ,it is appeared that the system is fitted to use when sending two bits as indicated in Table (1).

Table (1) Final design summary when sending 2-bit.

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	88	11,776	1%	
Number of 4 input LUTs	2,271	11,776	19%	
Logic Distribution				
Number of occupied Slices	1,255	5,888	21%	
Number of Slices containing only related logic	1,255	1,255	100%	
Number of Slices containing unrelated logic	0	1,255	0%	
Total Number of 4 input LUTs	2,352	11,776	19%	
Number used as logic	2,271			
Number used as a route-thru	81			
Number of bonded IOBs	6	372	1%	
Number of GCLKs	1	24	4%	
Number of MULT18X18SIOs	20	20	100%	
Total equivalent gate count for design	24,078			
Additional JTAG gate count for IOBs	288			

When increase the number of sent bits like to three, it is fitted as an utilization as Shown in Table (2) but when implemented gives a comment as shown in Figure (12).

Table (2) Final design summary when sending 3-bit

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	11,906	11,776	101%	OVERMAPPED
Logic Distribution				
Number of occupied Slices	6,621	5,888	112%	
Number of Slices containing only related logic	6,232	6,621	94%	
Number of Slices containing unrelated logic	389	6,621	5%	
Total Number of 4 input LUTs	12,642	11,776	107%	OVERMAPPED
Number used as logic	11,906			
Number used as a route-thru	736			
Number of bonded IOBs	8	372	2%	
Number of MULT18X18SIOs	20	20	100%	

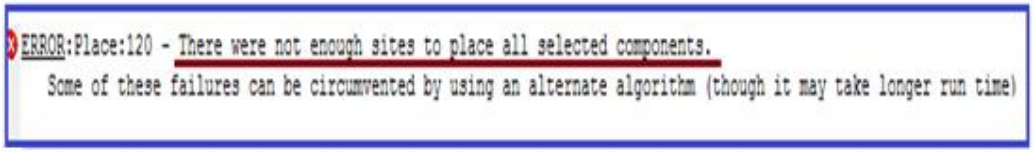

Figure (12) Implementation Error.

When send four bits it appears that it's not fitted because this will increase the number of circuit used as shown in Table (3), and when implemented gives a comment as shown in Figure (13) .

Table (3)Final design summary when sending 4-bit.

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	4932	5888	83%
Number of 4 input LUTs	9283	11776	78%
Number of bonded IOBs	6	372	1%
Number of MULT18X18SIOs	20	20	100%

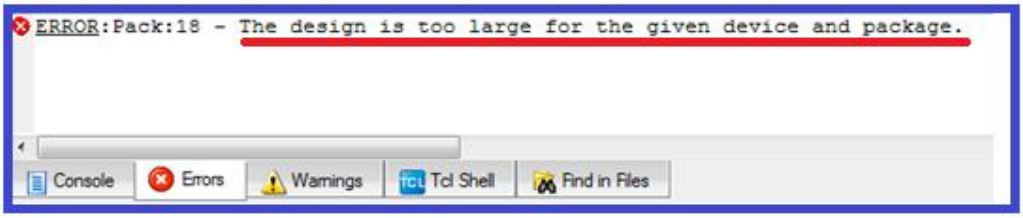

Figure (13) Implementation error.

FPGA IMPLEMENTATION

The implementation of MC-CDMA system on FPGA card is done by connecting the card to the PC as shown in Fig.(14) then after connecting the FPGA card Spartan-3A/AN ,it must specified the input and the output to the system and it specified by choose the inputs two slide switches and the outputs discrete led as shown in Figure (15).

Figure (14) Connecting the card.

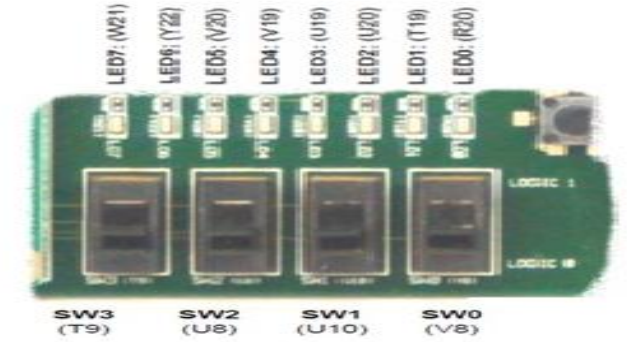

Figure (15) Assigning the input and the output.

Now the input is specified as [SW0 -SW1] and the output is specified as [LED0-LED1] , by assigning the bits for the input and the output the card will be ready to accept the system ,it mean ready for downloading the bit stream file for the system after choosing the bit file and programming it ,if the programming operation is done without error the PC will give an indication as shown in Figure (16) , the card now is programmed to transmit two bit from the transmitter to the receiver as shown in Figure (17).

Figure (16) the programming of the system on FPGA.

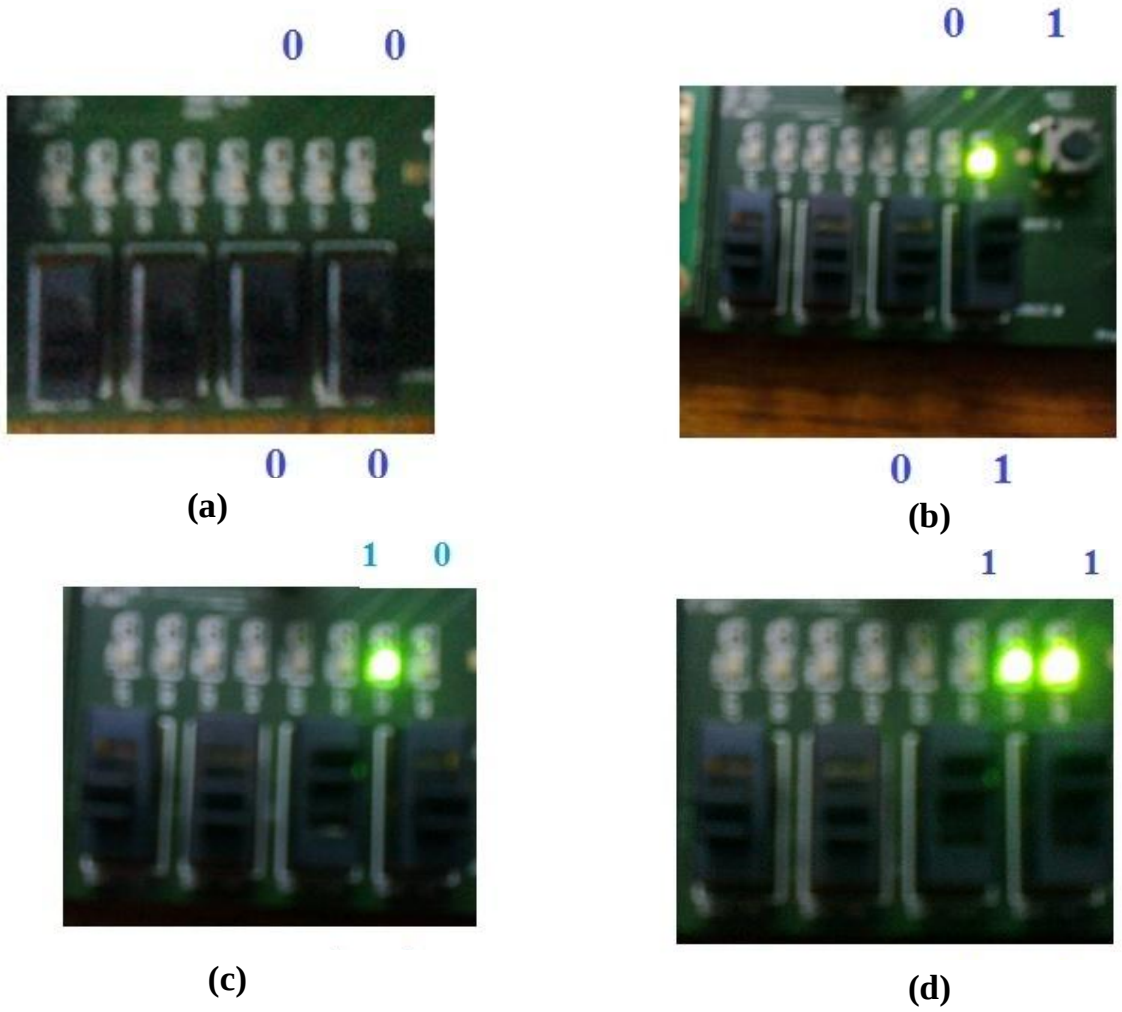

Figure (17) (a) Case (1) when bits=00 (b)Case (2) when bits=01 (c)Case (3) when bits=10 (d) Case (4) when bits=11.

CONCLUSIONS

A baseband MC-CDMA system was successfully developed using Spartan-3A/3AN, XC3S700N-3FGG484 FPGA of Xilinx family FPGA development board .The description was made by VHDL in Xilinx ISE the functionality was verified by Xilinx ISE 9.2i Edition. It can be seen that when sending two bit from the transmitter to the receiver the system has no problem to be implemented and downloaded on the FPGA device but when increasing to three bits it can be synthesized but cannot be implemented due to the indication given from the program that there is no enough sites to all components ,and finally when increased to four bit it cannot be synthesized due to the indication in the design summary that the system is overmapped and it cannot be implemented on the desired device .The

implemented design gives an easy way to increase the number of bits transmitted from the transmitter side by doing some modifications on the VHDL programming files that maintain the ability to reprogram and reconfigure FPGA devices.

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