Design and FPGA Implementation of Two-Dimensional Discrete Wavelet Transform Architectures Using Raster-Scan Method

Jassim M. Abdul-Jabbar  
Zahraa Talal Abed Al-Mokhtar  
Dept. of Computer Eng., College of Eng., University of Mosul, Mosul, Iraq  
drjssm@gmail.com  
zah_ta84@yahoo.com

Abstract

In this paper, an FPGA implementation of a 2-dimensional discrete wavelet transform (2-D DWT) is proposed to efficiently construct the corresponding two-dimensional architecture by using the raster-scan image method for any given hardware architecture of one dimensional (1-D) wavelet transform filter. The proposed method is based on lifting scheme architecture. The resulting architectures are simple, modular and regular for computation of one or multilevel 2-D DWT. These architectures perform both low pass and high pass filter with multiplierless coefficients calculation. In addition they require a small on-chip area to download the architectures on FPGA Board (Spartan-3E). The proposed 2-D architecture consists of: external memory, Row 1-D arithmetic module, column 1-D arithmetic module and internal memory unit. The row and column 1-D arithmetic units are designed utilizing Biorthogonal filters (5/3 and 9/7).

Keywords: 2-D DWT, FPGA implementation, Lifting scheme architecture, Raster-scan method.

التصميم والتنفيذ باستخدام FPGA للتحويل المويجي المتقطع ذي البعدين بطريقة المسح النقطي

د. جاسم محمد عبد الجبار
قسم هندسة الحاسوب .. كلية الهندسة .. جامعة الموصل .. الموصل .. العراق
zah_ta84@yahoo.com  
drjssm@gmail.com

الخلاصة

في هذه البحث، تم اقتراح تنفيذ بنية التحويل المويجي المتقطع ذي البعدين (2-D DWT) باستخدام FPGA بكفاءة من خلال إنشاء صورة المسح النقطي لأي بنية مادية للتحويل المويجي ذات البعدين الواحد (1-D). تستخدم الطريقة المقترحة على معمارية مخطط الرفع. البنية الناتجة كانت سهلة ومدمجة ومتعددة مستويات واحدة أو اثنين من التحويل المويجي المتقطع ذي البعدين (2-D DWT). هذه البنية يمكنها تنفيذ عمليات مرشح الإمرار الواصلة ومرشح الإمرار العالي مع إجراء الحساب للمعاملات بدون مضارب. بالإضافة إلى ذلك فإنها تتطلب مساحة صغيرة على رقاقة FPGA نوع (Spartan-3E). ينتمي الهيكل ذي البعدين المقترح: الدائرة الخارجية ووحدة حساب الصف ذات البعدين الواحد ووحدة حساب العمود ذات البعدين الواحد بالإضافة إلى وحدة الذاكرة الداخلية ذات البعدين الواحد المصممة للفحص والمزدوج باستخدام مرشحات (5/3 و 9/7) ثنائية التعمام.
1. Introduction

The discrete wavelet transform (DWT) is developed as an effective tool for multiresolution analysis since its first presentation by Mallat [1] due to its good time-frequency characteristics. The DWT is widely used for signal and image analysis. The direct implementation of DWT usually requires heavily arithmetic computations because it is essentially a two-channel filter bank (i.e. convolution method). Lifting scheme is latest efficient way to reduce the arithmetic complexity and to provide an in place implementation [2]. For 2-D DWT, there are many VLSI architectures [3] - [7]. The direct method of 2-D DWT architecture performs 1-D DWT on the every row and then on every column of the image. However, this architecture needs a frame buffer as shown in Fig.1 which is usually an off –chip to store the intermediate data [8]. The external memory access consumes the most power in the 2-D DWT hardware implementation. The systolic architecture may be preferred because of the smaller external memory access. But this architecture requires some internal line buffer and processing elements which increase the die area and control complexity [6]. In this paper, a simple method is proposed to implement separable 2-D raster-scan image architectures to solve the problem of internal memory access.

The basic idea is based on utilizing 2-Data buffer to store the approximation and detail coefficients. These architectures are flexible and can be used for many filter kinds. Based on lifting scheme method, a 1-D arithmetic module is used to build the 2-D DWT for one and multilevel transformation. The 2-D DWT architectures are designed to perform the one and multilevel using biorthogonal 5/3 filter & 9/7 filters.

The rest of this paper is organized as follows; The lifting scheme analysis is given in section 2. The 1-D arithmetic modules for 5/3 and 9/7 filters are presented in section 3. In section 4, the proposed architectures are explained. The simulation result and hardware requirement are illustrated in section 5 and 6, respectively. The comparison of the proposed architectures with other architectures of recent studies is shown in section 7. Finally, section 8 concludes this paper.

2. Lifting-Based DWT

The lifting schemes consist of 3-steps as shown in Fig. 2 [9]:
1- Split step: - the input signal is separated into even and odd samples.
2- Predict step: - the even samples are multiplied by the time-domain equivalent of t(z) and then added to odd samples.
3- Update step: - the predict samples are multiplied by time-domain equivalent s(z) and then added to even samples.
The basic principle of the lifting scheme is to factorize the polyphase matrix of wavelet filter into a sequence of alternating upper and lower triangular matrices and diagonal matrices [9]. The corresponding polyphase matrices are defined by the following matrix equation [4]:

\[
\tilde{P}(z) = \prod_{k=1}^{n} \begin{bmatrix} 1 & s(z) \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ t(z) & 1 \end{bmatrix}.
\] (1)

\(\tilde{P}(z)\) is defined as polyphase matrix of decomposition stages.

### 2.1 Lifting scheme for 5/3 filter

The filter coefficients of 5/3 filter are defined as [10]

Low pass decomposition filter \(h(n) = [-1/2 \ 1 \ -1/2]\).

High pass decomposition filter \(g(n) = [-1/8 \ 1/4 \ 3/4 \ 1/4 \ -1/8]\).

The polyphase matrix of the above filter is

\[
\tilde{P}(z) = \begin{bmatrix} -1/8 & Z + 3/4 \ -1/8 & Z^{-1} \\ -1/2 & -1/2 & Z^{-1} & 1 \end{bmatrix}.
\]

\[
\tilde{P}(z) = \begin{bmatrix} 1 & 1/4 (1 + Z) \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ -1/2(1+Z^{-1}) & 1 \end{bmatrix}.
\] (2)

So the approximation and detail coefficients are respectively defined by [13]

\[
d(2n+1) = x(2n+1) + \alpha [x(2n) + x(2n+2)]
\] (3)

and

\[
a(2n) = x(2n) + \beta [d(2n+1) + d(2n-1)]
\] (4)

where \(\alpha = -1/2\), \(\beta = 1/4\).

### 2.2 Lifting scheme for 9/7 filter

For a 9/7 symmetric biorthogonal perfect reconstruction (PR) filter, \(h(k) = h(-k)\) and \(g(k)=g(-k)\); for \(k = 0; 1; 2; 3; 4\). [11]. Then the even and the odd parts of them can be written as

\[
h_e(z) = h(0) + h(2)(z + z^{-1}) + h(4)(z^2 + z^{-2})
\] (5a)

and

\[
h_o(z) = h(1)(1 + z) + h(3)(z^2 + z^{-1})
\] (5b)

with

\[
g_e(z) = -h_o(z^{-1})
\] (6a)

and

\[
g_o(z) = h_e(z^{-1})
\] (6b)
2.2.1 Lifting factorization of the 9/7(PR) filter

(i) When $h(3) \neq 0$. [11]

By virtue of Euclidean algorithm, let

$$he(z) = h_0(z)*q_1(z) + r_1(z)$$

then we have

(a) $q_1(z) = s_0(1 + z^{-1}); r_1(z) = t_1(z + z^{-1}) + t_0$

where

$$s_0 = h(4)/h(3)$$

$$t_0 = h(0) - [2h(1)*h(4)]/h(3)$$

and

$$t_1 = h(2) - h(4)-[3h(1)*h(4)]/h(3).$$

(b) $h_0(z) = r_1(z)*q_2(z) + r_2(z)$

$$q_2(z) = s_1 (1 + z)$$

$$r_2(z) = t_2 (z + 1)$$

where

$$s_1 = h(3)/t_1$$

and

$$t_2 = h(1) - h(3) - [t_0*h(3)]/t_1$$

(c) $r_1(z) = r_2(z)*q_3(z) + r_3(z)$

Also

$$q_3(z) = s_2 (1 + z^{-1})$$

$$r_3(z) = t_3$$

where

$$s_2 = t_1/t_2$$

$$t_3 = t_0 - 2t_1$$

(d) $r_2(z) = t_3*s_3(z+1)$

and

$$q_4(z) = s_3(1 + z)$$

$$r_4(z) = 0$$

where

$$s_3 = t_2/t_3.$$

The above process can be summarized as in the following lifting factorization, where the polyphase matrix of the decomposition stage is defined as

$$\tilde{P}(z) = \begin{bmatrix} h_{0e}(z) & h_{o0}(z) \\ g_{1e}(z) & g_{10}(z) \end{bmatrix}$$

The above equation can be rewritten as

$$\tilde{P}(z) = \begin{bmatrix} 1 & s_0(1 + z^{-1}) \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ s_1(1 + z^{-1}) & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & s_2(1 + z^{-1}) \\ s_3(1 + z^{-1}) & 1 \end{bmatrix}$$
2.2.2 Construction of the 9/7 wavelet filter

It is necessary to point out that, for any given filter coefficients \( h(k)= h(-k) \) and \( g(k)=g(-k); \) [11] they need not be wavelet filters. In fact, in order to achieve the 9/7 wavelet filter, may be calculated using the vanishing moments that satisfy \( M=2 \) and \( M=4, \) can be calculated using

\[
\begin{align*}
   h^{(k)}(z) \big|_{z=1} &= 0, \quad k=0,1 \quad \text{and} \\
   g^{(k)}(z) \big|_{z=1} &= 0, \quad k=0,1,2,3
\end{align*}
\]

Rewriting (15) as

\[
\begin{align*}
   \tilde{P}(z) &= \left[ \begin{array}{cc}
      1 & \alpha (1+Z^{-1}) \\
      0 & 1
   \end{array} \right] \left[ \begin{array}{cc}
      1 & 0 \\
      \beta (1+Z) & 1
   \end{array} \right] \left[ \begin{array}{cc}
      1 & \gamma (1+Z^{-1}) \\
      0 & 1
   \end{array} \right] \\
   &= \left[ \begin{array}{cc}
      1 & 0 \\
      0 & 1
   \end{array} \right] \left[ \begin{array}{cc}
      \delta (1+Z) & 0 \\
      \zeta & 1/\zeta
   \end{array} \right]
\end{align*}
\]

Based on the vanishing moments conditions and normalization conditions \( h(1)= 2; \) \( g(1)= 1, \) and comparing (15) and (16), different coefficients can be evaluated as

\[
\begin{align*}
   \alpha &= (-2t+1)/4(t-1) \\
   \beta &= - (t-1)^2 \\
   \gamma &= 1/(4t(t-1)) \\
   \delta &= \zeta = 2/t \\
   \zeta &= \zeta = 2/t
\end{align*}
\]

From (16) and (17), symmetric biorthogonal 9/7 filters can be obtained with a free parameter \( t. \) In other words, for any real parameter \( t, \) (16) and (17) can be used for signal decomposition, where \( h \) and \( \tilde{h} \) denote low pass filters, and \( g \) and \( \tilde{g} \) denote high pass filters for analysis and synthesis, respectively. In order to achieve the 9/7 symmetric biorthogonal wavelet filter, Daubechies’s theorem can be employed to determine the interval that the parameter \( t \) can be included. Firstly, denote \( h_9(z) \) and \( \tilde{h}_7(z) \) by [11]

\[
\begin{align*}
   h_9(z) &= \left((1+z^{-1}/2)^2 \right) F(z) \\
   \tilde{h}_7(z) &= \left((1+z^{-1}/2)^2 \right) Q(z)
\end{align*}
\]

Taking \( t = 1.25; \) then the coefficients of the 9/7 wavelet filter are given by

\[
\begin{align*}
   \{h(0), h(1), h(2), h(3), h(4)\} &= (1/10) \times \{190/16, 86/16, 24/16, 6/16, 9/16\} \\
   \{g(0), g(1), g(2), g(3)\} &= \{18/32, 19/64, -1/32, -3/64\} \\
   h(-k) &= h(k) \quad \text{and} \\
   g(-k) &= g(k)
\end{align*}
\]

3. The Proposed Arithmetic Module

3.1 1-D arithmetic module

The proposed architecture contains the two dimensional forward discrete wavelet transform (2-D FDWT) and the two dimensional inverse discrete wavelet transform (2-D IDWT). It calculates in row–column fashion on the NXN image by using Biorthogonal filters (5/3 & 9/7 filter)). Such architecture consists of: Row 1-D DWT arithmetic module, memory unit, and column 1-D DWT arithmetic module. Note that the forward discrete
wavelet transform (FDWT) and the inverse discrete wavelet transform (IDWT) are symmetrical. In the remaining parts of this paper, all the details are discussed in terms of discrete wavelet transform modeling by using (5/3, 9/7) filters.

3.1.1 1-D DWT arithmetic module for 5/3 filter

The 1-D DWT module of lifting scheme can be naturally pipelined as shown in Fig. 3 [13].

Since such module uses multipliers and adders, another 1-D DWT arithmetic module using pipelining of shift integer adder is proposed as shown in Fig. 4. The pipeline structure reduces the area cost of the architecture as compared with the multiplier arithmetic module and reduces the worst delay path between registers.

The proposed 1-D DWT arithmetic module in 5/3 filter consists of two stages; the first stage is used to calculate the detail coefficient and the second stage calculates the approximation coefficient as shown in Fig. 5. So each stage has three input signals and two data output signals.
3.1.2 1-D DWT arithmetic module for 9/7 filter

In this paper, the 9/7 filters are designed as 4-stage pipelined shift integer adder without using any multipliers as shown in the Fig. 6. Depending on equation (9). So the 9/7 filter can be designed as two blocks, each block is a 5/3 filter pipelined -shift integer adder module with a simple change in block 1 as shown in Fig. 7.

![Diagram of 1-D DWT arithmetic module for 9/7 filter](image-url)
In 5/3 filter, the 1-D DWT arithmetic module consists of three input signals and two output signals. In 9/7 1-D DWT arithmetic module, block 1 consist of three input signals and three output signals, while the block2 in 9/7 module, is exactly the arithmetic module in 5/3 filter. So, the 1-D DWT arithmetic module in 9/7 filter can be designed using two 1-D DWT arithmetic modules in 5/3 filter as shown in Fig. 8.

4. The Proposed FPGA Implementation

4.1 The proposed 1-level architectures

The proposed architecture performs 2-D DWT on the input signal (image) by using row-column fashion, so it is required to use three arithmetic modules to calculate the lifting scheme. One of these arithmetic modules is used to calculate the 1-D DWT for each row in the image and the others are used to calculate the 1-D DWT for each column in the image.

As shown in Fig. 9, The input data (image NXN) must be read as raster scan (i.e. row by row) from external memory, the first row of the image is read from an external memory and stored in the Memory unit 1 (MEM1). After that, the row 1-D arithmetic module of 5/3 filter (block 1) reads three input signals from MEM1, calculates the approximation and detail coefficients and stores the results in MEM2. These operations are repeated until the last pixel of the first row. The second row of the image is stored in MEM1 and the row 1-D arithmetic module of 5/3 filter performs the same operations to calculate the approximation and the detail coefficients of the second row which are stored in MEM3 as shown in Fig. 9. Note that the column 1-D arithmetic module2 (block2) and column 1-D arithmetic module3 (block3) are not shown in Fig. 9.
arithmetic module3 (block3) are not used until this time. When first two coefficients are stored in MEM3, block2 and block3 begin to work by performing the lifting scheme on every column of the image. Block2 reads the approximation coefficients from MEM2 and MEM3 and calculates the sub-band images (LL, LH) and block3 reads the detail coefficients from MEM2 and MEM3 to calculate the sub-band images (HL, HH). Such operations continue until the last pixel of the image. The same structure of Fig. 9 can be used for 9/7 filters, where each of block1, block2 and block3 are replaced by the corresponding 1-D arithmetic module of 9/7 filter instead of the shown 5/3 module.

![Diagram](image-url)

**Fig. (9): A one level raster-scan 2-D DWT architectures by using 5/3 filter.**

### 4.2 The proposed multilevel architectures

The proposed 1-level architectures can be easily extended to the multilevel architectures by using the following two methods:

**Method 1:** using the proposed 1-level architecture and storing, LL sub-band image in an external memory. When the first level finishes, the same processing element (1-level proposed architecture) reads the LL sub-band image. This process needs the use of the external memory. This will increase the time delay and increase the external memory access but the die area need to build this method will be small.

**Method 2:** using n-time of the 1-level proposed architecture, where n is the number of levels. In this paper, the architectures are designed via this method to perform the 3-level 2-D DWT. This method needs a die area in FPGA board greater than the method 1, but method 2 reduces the external memory access and the output from level 2 and level 3 can be used immediately. The multilevel architecture for method 2 is as shown in Fig. 10.

### 5. Simulation Results

In order to determine the number of bits required for representing each signal, two lengths must be determined. The length of real part (m1) and the length of mantissa part (m2) as shown in Fig. 11. The number of bits for mantissa representation turns out to be the critical parameter for the design. In the proposed architectures, to find the minimum
values of $m_1$ and $m_2$ with reasonable high image quality as shown in Table 1, a Matlab code for a set of standard images is performed. From Table 1, the real part consists of 8 bits in both (5/3 filter and 9/7 filter) architectures, but the mantissa part in (5/3 filter) architectures is 4 bits and the mantissa part in (9/7 filter) is 9 bits.

<table>
<thead>
<tr>
<th>Images</th>
<th>Filter</th>
<th>SNR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lena 512 X512</td>
<td>5/3 filter</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td>9/7 filter</td>
<td>39</td>
</tr>
<tr>
<td>Barbara 512X512</td>
<td>5/3 filter</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td>9/7 filter</td>
<td>36</td>
</tr>
<tr>
<td>Goldhill 512X512</td>
<td>5/3 filter</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td>9/7 filter</td>
<td>36</td>
</tr>
</tbody>
</table>

Fig. 10 The proposed multilevel architecture.

Fig. 11 The total number of bits required for representing each signal for 5/3 and 9/7 filters.

Table 1 The most proper SNR values to determine the total number of bits.
6. Hardware Implementation

After achieving satisfactory results from Matlab simulation in the previous section, we proceed to the next stage where the codes are translated into VHDL. Then, the VHDL codes are synthesized using the synthesis tool, which produces “gate level” architecture for VLSI implementation. Finally, the design is downloaded into the FPGA board (Spartan-3E) for the functionality verification. The synthesis results are presented in Table 2.

<table>
<thead>
<tr>
<th>Architectures</th>
<th>Available slices</th>
<th>Number of slices</th>
<th>Max. frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed 1-level 2D DWT for 5/3 filter</td>
<td>46</td>
<td>4656</td>
<td>196 MHz</td>
</tr>
<tr>
<td>Proposed 1-level 2D DWT for 9/7 filter</td>
<td>57</td>
<td>4656</td>
<td>178.3 MHz</td>
</tr>
<tr>
<td>Proposed multilevel (3 levels) architecture for 5/3 filter</td>
<td>210</td>
<td>4656</td>
<td>96.4 MHz</td>
</tr>
<tr>
<td>Proposed multilevel (3 levels) architecture for 9/7 filter</td>
<td>285</td>
<td>4656</td>
<td>100.2 MHz</td>
</tr>
</tbody>
</table>

7. A Comparative Study

The proposed design can implement a 2-D multilevel lifting scheme discrete wavelet transform concurrently. It does not use any external memory to store the intermediate results. This will avoid the delay caused by the memory access. As illustrated in Table 3, the design of 1-level of raster-scan 2-D DWT architecture for 5/3 filter requires 12 adders and 9 shift registers, without any multiplier. The multilevel (3 levels) architecture requires 36 adders and 27 shift registers. For 9/7 architectures, the 1-level raster-scan 2-D DWT requires 36 adders and 54 shift registers, while multilevel architectures require 108-adder and 162 shift registers.

<table>
<thead>
<tr>
<th>Architectures</th>
<th>Number of adder</th>
<th>Number of shift register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed 1-level 2D DWT for 5/3 filter</td>
<td>12</td>
<td>9</td>
</tr>
<tr>
<td>Proposed 1-level 2D DWT for 9/7 filter</td>
<td>36</td>
<td>27</td>
</tr>
<tr>
<td>Proposed multilevel (3 levels) architecture for 5/3 filter</td>
<td>36</td>
<td>54</td>
</tr>
<tr>
<td>Proposed multilevel (3 levels) architecture for 9/7 filter</td>
<td>108</td>
<td>162</td>
</tr>
</tbody>
</table>

It should be noted that the direct structure uses 4-multipliers and 8 adders [12], while the flipping structure reduces the critical path by releasing the major computation path, but without any hardware overhead [10]. The internal memory size in both direct architecture and flipping architecture is equal the image size (NXN). The proposed architectures need internal memory less than image size as shown in Table 4. This will reduce the complexity of the system because the proposed architectures do not need the memory control unit.
Table (4): A comparison of the 2-D architectures for different architectures.

<table>
<thead>
<tr>
<th>Architectures</th>
<th>No. of multipliers</th>
<th>No. of adders</th>
<th>Internal memory</th>
<th>Control complicity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Direct</td>
<td>4</td>
<td>8</td>
<td>NXN</td>
<td>Complex</td>
</tr>
<tr>
<td>Flipping</td>
<td>4</td>
<td>8</td>
<td>NXN</td>
<td>Simple</td>
</tr>
<tr>
<td>Proposed 1-level raster scan 2D DWT for 5/3 filter</td>
<td>0</td>
<td>12</td>
<td>3N+2</td>
<td>Simple</td>
</tr>
<tr>
<td>Proposed 1-level raster scan 2D DWT for 9/7 filter</td>
<td>0</td>
<td>36</td>
<td>3N+8</td>
<td>Simple</td>
</tr>
<tr>
<td>Proposed multilevel-level (3levels ) architecture for 5/3 filter</td>
<td>0</td>
<td>36</td>
<td>7N+6</td>
<td>Simple</td>
</tr>
<tr>
<td>Proposed multilevel-level (3levels ) architecture for 9/7 filter</td>
<td>0</td>
<td>108</td>
<td>7N+24</td>
<td>Simple</td>
</tr>
</tbody>
</table>

8. Conclusions

This paper has presented a high performance and low memory raster-scan architectures for the 2-D lifting scheme DWT of the 5/3 filter and 9/7 filters. By merging predict and update steps into a single step. The proposed architectures use 3-arithmetic module in 1-level architectures and 9 arithmetic modules in multilevel architectures without any multipliers. The proposed scheme in this paper depends on lifting scheme theory because it is a desirable scheme from point of view of hardware performance and high throughput. The proposed 1-level and multilevel 2-D DWTs have been designed, implemented and tested. The comparison shows that the proposed architectures are also preferable from chip utilization point of view.

References

[8] C. Hung, P. Tseng and L. Chen “Generic RAM-based architectures for two dimensional discrete wavelet transform with line-Based method” IEEE. Transactions on

The work was carried out at the college of Engineering, University of Mosul