

A 2.4 GHz Differential Class-E Power Amplifier with on-Chip Transformers for Bluetooth Systems

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ABSTRACT:

This work presents the design and simulation of a differential class-E Power Amplifier (PA) for class-1 Bluetooth systems in 0.13 μm RF CMOS technology. The proposed PA can deliver 21.57 dBm output power to a 50 Ω load at 2.4 GHz with 65.59 % Power-Added-Efficiency (PAE) from 1 V supply voltage. In order to achieve fully integrated PA, on-chip balun transformers are designed and improved for converting single-ended input signal to differential signal in the input side and differential signal to single-ended output signal in the output side. The results are obtained using microwave office 2009 (version 9.00).

Keywords: RF power amplifier, class-E, Bluetooth, CMOS technology, on-Chip balun transformer.

مضخم قدرة (2.4 GHz) تفاضلي صنف E مع محولات على الرقاقة لانظمة بلوتوث

الخلاصة

هذا البحث يقدم التصميم والمحاكاة لمضخم قدرة (2.4 GHz) تفاضلي صنف E لانظمة بلوتوث من الصنف الاول منفذة بتقنية CMOS باجراء (0.13 μm). يوفر المضخم المقترح قدرة خرج (21.57 dBm) وكفاءة قدرة مضافة PAE تساوي (65.59 %) عند تردد (2.4 GHz) بأستخدام مجهز (1 V). كما تم تصميم وتحسين محولات على الرقاقة وذلك لتحقيق تكامل كلي لتصميم مضخم القدرة المقترح. هذه المحولات تستخدم كوسيلة لتحويل الإشارة احادية النهاية الى إشارة تفاضلية في جهة الادخال والعكس في جهة الاخراج. تم الحصول على النتائج باستخدام برنامج المحاكاة (Microwave Office 2009).

INTRODUCTION

The Bluetooth is recognized as an industry standard for short-range data and voice transfer to link mobile phones, laptops, digital cameras, and other portable devices [1]. It is considered to be a high speed, low cost wireless technology, working with a radio frequency band (called the industrial, scientific, and medical bandor (ISM) for the short) between 2.4-2.48 GHz. This frequency band is free for anyone to use, for any purpose (unlicensed) [2]. For Bluetooth applications, there are basically three classes based on the transmission distance (100, 10, and 1-meter range), they are Class 1 (The transmitted output power

is 20 dBm), Class 2 (The transmitted output power is 4 dBm) and Class 3 (The transmitted output power is 0 dBm), respectively [3].

Today, wireless applications like Bluetooth, WLAN etc. are rapidly growing and there is the need for low cost and high efficiency power amplifier [4]. The design of an on-chip front-end power amplifier with high power efficiency in the mainstream Complementary Metal-Oxide-Semiconductor (CMOS) technology is a challenging problem [5]. The difficulty of CMOS power amplifier lies in the design, including the low breakdown voltage of active devices and low supply voltage. So far, the differential topology has been widely considered as the one of the best solution, and it features a virtual ground, which can cancel the even harmonics. Besides, it will reduce the disturbance to other blocks in the transceiver when it is fully integrated in the system [6].

Since the modulation scheme employed by Bluetooth is Gaussian Frequency Shift Keying (GFSK), which is a constant envelope modulation scheme, a switching-mode (non-linear) PA can be used to achieve high efficiency. Among all classes of nonlinear power amplifiers, the class-E power amplifier is better choice in terms of circuit simplicity and high efficiency and this class has good performance at higher frequency [7].

Murad et al., 2010 [8] presented a 2.4 GHz CMOS single-ended PA for wireless applications in TSMC 0.18 μm CMOS technology. All circuit components, except the output matching network, have been designed on chip. The power amplifier delivered an output power of 19.2 dBm with a PAE of 27.8 % from 3.3 V power supply. Meshkinet al., 2010 [7] designed a switch-mode CMOS class-E power controllable PA suitable for modern wireless communications in TSMC 0.18 μm CMOS process. The designed PA can deliver 21.09 dBm output power to 50 Ω load at 2.4 GHz with 57 % PAE from 1.8 V supply voltage and the output power can be controlled in 1 dBm steps with small drop in efficiency. Chen et al., 2011 [3] described the design of the two stage of class-E power amplifier for class 1 Bluetooth applications in 0.18 μm CMOS technology with load mismatch protection and power control features. Power control was realized by means of "open loop" techniques to regulate the power supply voltage. Post-layout simulation a 25.1 dBm output power and 54.2 % PAE were achieved at a nominal 1.8 V supply voltage. Raza and Jonas, 2013 [9] presented a novel approach of implementing parallel circuit differential class-E amplifier. A test circuit is implemented in 0.13 μm CMOS process. The power amplifier achieves 22 dBm output power at 2.4 GHz from a 2.5 V with an overall PAE of 38 %.

The outline of this paper is as follows. In section 2, the design of a differential class-E PA for class 1 Bluetooth application with two ideal transformers is described. In section 3, the design of on-chip transformers is demonstrated. The simulation results are presented in section 4. Finally, in section 5, conclusions are given.

DESIGN OF A DIFFERENTIAL CLASS-E PA WITH TWO IDEAL TRANSFORMERS

The design starts with the single-ended class-E PA followed by the differential configuration with two ideal transformers as following:

The circuit topology (basic circuit) of a class-E power amplifier is shown in Figure (1) [10]. In this circuit L_1 represents the drain bias RF choke, V_{dd} is the drain supply voltage, C_s is the capacitor shunting the active device (Q_1), L_s is the class inductance, L_{os} and C_{os} constitute a series resonant circuit tuned at the operating frequency, L_x is the excess (resultant) inductance and R_s is the optimum resistance

seen by the load network for the required output power. The active device, Q_1 , (MOSFET in this case) operates as an ON/OFF switch.

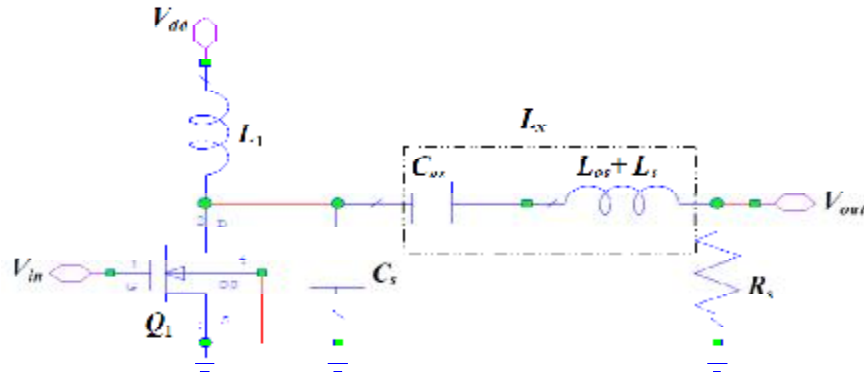


Figure (1): Typical class-E power amplifier with shunt capacitance configuration.

The component values of the circuit in Figure 1 are calculated at output power $P_{out} = 50$ mw (17 dBm), operating frequency $f_o = 2.4$ GHz, loaded quality factor $Q_{Ls} = 10$ and drain supply voltage = 1 V using the following equations [10]:

$$C_s = \frac{P_{out}}{\pi * \omega_o * V_{dd}^2} \quad \dots (1)$$

$$R_{s(opt)} = 0.577 \left(\frac{V_{dd}^2}{P_{out}} \right) \quad \dots (2)$$

$$L_x = \frac{\pi * V_{dd}^2 (\pi^2 - 4)}{2 * \omega_o * P_{out} (\pi^2 + 4)} \quad \dots (3)$$

where $\omega_o = 2\pi f_o$.

The value of L_1 can be calculated by the resonant equation of an LC tank as follow:

$$L_1 = \frac{1}{\omega_o^2 C_1} = \frac{1}{\omega_o^2 (C_p - C_s)} \quad \dots (4)$$

where

- C_1 : the cancelation capacitance by the inductor,
- C_p : exact shunt capacitance at the drain of the transistor, and
- C_s : capacitance of the class.

In order to match a 50Ω load, an up-conversion matching network is implemented to transform an optimum load to a 50Ω load. L-matching network is chosen because of its circuit simplicity. Also, the excess inductance (L_x) in a class-E power amplifier can be combined with the inductor used in the matching network if a low-pass L matching network is used. Therefore, the schematic of a class-E power amplifier is modified as shown in Figure (2).

The values of L_m , C_m and L_{total} can be calculated using the following equations [11]:

$$L_m = \frac{\sqrt{R_{opt} (R_L - R_{opt})}}{\omega_o} \quad \dots (5)$$

$$C_m = \frac{\sqrt{(R_L - R_{opt})/R_{opt}}}{\omega_o} \quad \dots (6)$$

$$L_{total} = L_x + L_m \quad \dots (7)$$

Using Equation (1) to Equation (7), the calculated component values for single-ended class-E power amplifier are summarized in Table (1).

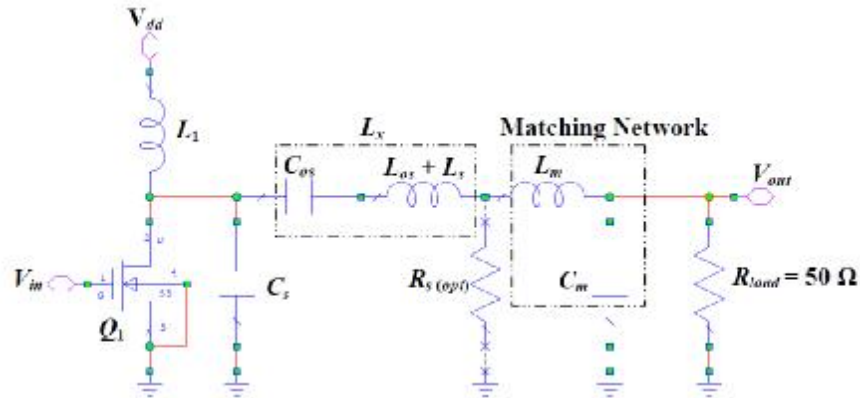


Figure (2): Complete schematic (single-ended) of a class-E power amplifier.

Table (1): Component values of the single-ended class-E PA.

Component	Value	Unit
C_s	0.73	pF
$R_{s(opt)}$	16.60	Ω
L_1	2.00	nH
L_x	1.26	nH
L_m	1.56	nH
C_m	1.87	pF
L_{total}	2.83	nH

The final step in the design is combining of two single-ended topology to produce differential topology and then using two ideal transformers, the first one in the input side is to convert single ended input signal to differential signal and the second in the output side is to convert the differential signal to single-ended 50 Ω load signal as shown in Figure (3). The additional objective of using ideal transformers is obtaining the primary results.

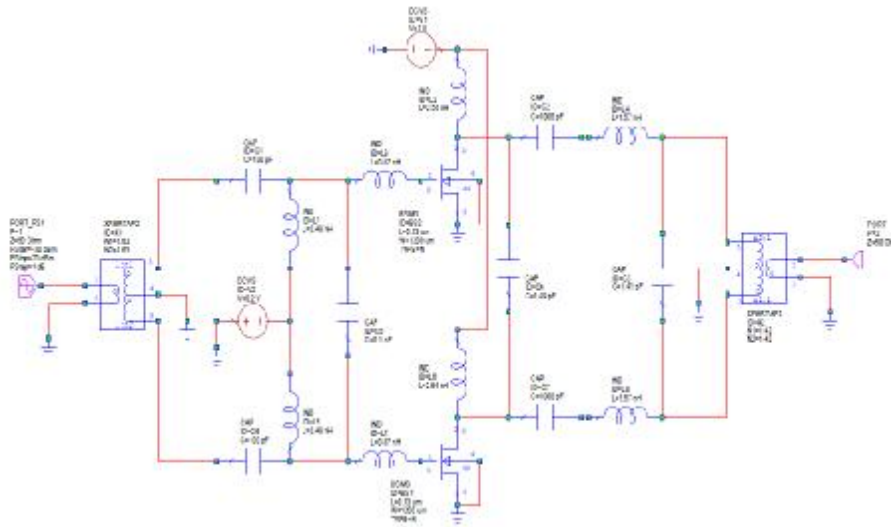


Figure (3): The proposed differential class-E power amplifier with two ideal transformers.

DESIGN OF ON-CHIP TRANSFORMERS

On-chip transformers contribute substantially in enhancing reliability, efficiency, and performance of silicon-integrated Radio-Frequency (RF) circuits. Many researchers have reported the integration of on-chip transformers in PAs [12]. In order to design on-chip transformers instead of the ideal transformers, which used with the proposed class-E PA of Figure 3, the inductance required for each winding of the transformer must be determined from consideration of the terminal impedances and center frequency specification. As a first step, L-section matching network that employed in the proposed design is converted to parallel section matching network as shown in Figure 4. In these networks L_1 represents the inductance of the primary winding, R_p is the parallel (differential) resistance, R_L is the output resistance, which is typically 50Ω , R_{opt} is the optimum resistance seen by the load network of the class-E PA and C_1 locates in parallel to the inductance.

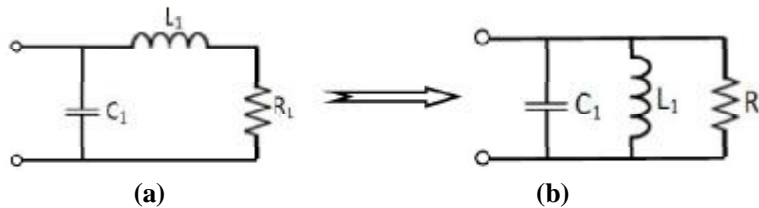


Figure (4): Matching networks, (a) L-section, (b) parallel section.

This conversion process is achieved using the following equations [13]:

$$R_p = R_{(differential)} \quad \dots (8)$$

$$R_{(differential)} = 2R_{(opt)} \quad \dots (9)$$

$$R_p = \frac{L_1^2 \omega_0^2}{R_L} \quad \dots (10)$$

$$C_1 = \frac{1}{L_1 \omega_0^2} \quad \dots (11)$$

According to the on-chip (1:1) square transformer, the value of the inductance for secondary winding can be calculated from:

$$n = \left(\frac{L_2}{L_1}\right)^{1/2} \dots(12)$$

In the proposed PA, the component values of the parallel matching network are calculated using Equation (8) to Equation (12), at load resistance $R_L = 50 \Omega$, operating frequency $f_o = 2.4 \text{ GHz}$, turn ratio $n = 1$, and the optimum resistance $R_{opt} = 16.6 \Omega$. The calculated values are summarized in Table (2).

Table (2): Component values of the Parallel matching network.

Component	Value	Unit
L_1	2.7	nH
L_2	2.7	nH
C_1	1.62	pF

The design of an on-chip transformer is dependent on the available process. Nonetheless, good efficiency of the transformer can be obtained by increasing the magnetic coupling factor (k) and improving the quality factor (Q) of the coupled inductors, that is; minimizing of the minimum insertion losses (IL_{min}). In order to improve coupling factor, the wide metal traces of the transformer can be split into multiple parallel segments and interleaved [14].

In the next step of the design, the dimensions of the transformer (outer dimension (D_{out}), width of primary and secondary traces (W_p, W_s)) are adjusted until the inductances for primary and secondary winding approaching to the values which calculated from matching network in Table (2). Virtually, for 1:1 square transformer with geometrical parameters that are illustrated in Table (3), the on-chip balun transformer (a device which converts a single ended (unbalanced) signal to a differential (balanced) signal and vice versa) is designed and optimized using the following design equations [14]:

$$Q_p = \frac{Im(Z_{11})}{Re(Z_{11})} \quad \text{and} \quad Q_s = \frac{Im(Z_{22})}{Re(Z_{22})} \dots (13)$$

$$k = \frac{\sqrt{Im(Z_{12}) \cdot Im(Z_{21})}}{\sqrt{Im(Z_{11}) \cdot Im(Z_{22})}} \dots (14)$$

$$IL_{min}(dB) = 10 \log_{10} \left[1 + \frac{2}{(K^2 Q_p Q_s)} + 2 \sqrt{\frac{1}{(K^2 Q_p Q_s)} \left(1 + \frac{1}{(K^2 Q_p Q_s)} \right)} \right] \dots(15)$$

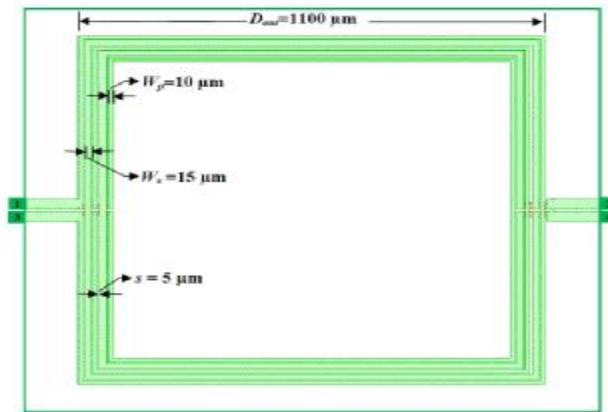
The primary and the secondary inductances can be calculated in terms of R_1 and R_2 , Q_1 and Q_2 for primary and secondary respectively, i.e.

$$L_1 = \frac{Q_1 R_1}{\omega_o} \quad \text{and} \quad L_2 = \frac{Q_2 R_2}{\omega_o} \dots(16)$$

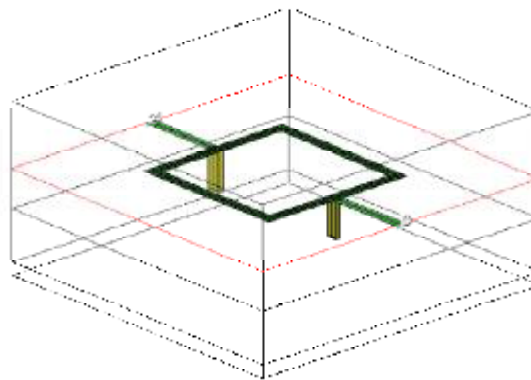
In this design, a standard 0.13 μm CMOS process with two aluminum metal layers is used. This process provides the top metal of 3 μm thickness and the dielectric thickness of 4 μm . Figure 5 shows the Electro-Magnetic Sight (EMSIght) setup for on-chip balun transformer.

Table (3): Geometrical parameters and simulation results for on-chip balun transformer.

Geometrical parameters		Simulation results	
$D_{out}(\mu\text{m})$	1100	$L_p(\text{nH})$	2.9
$W_p(\mu\text{m})$	10	$L_s(\text{nH})$	3.3
N_{seg}	3	Q_p	11.6
$W_s(\mu\text{m})$	15	Q_s	11.9
N_{seg}	2	K	0.7
$s(\mu\text{m})$	5	$IL_{min}(\text{dB})$	1.2



(a)

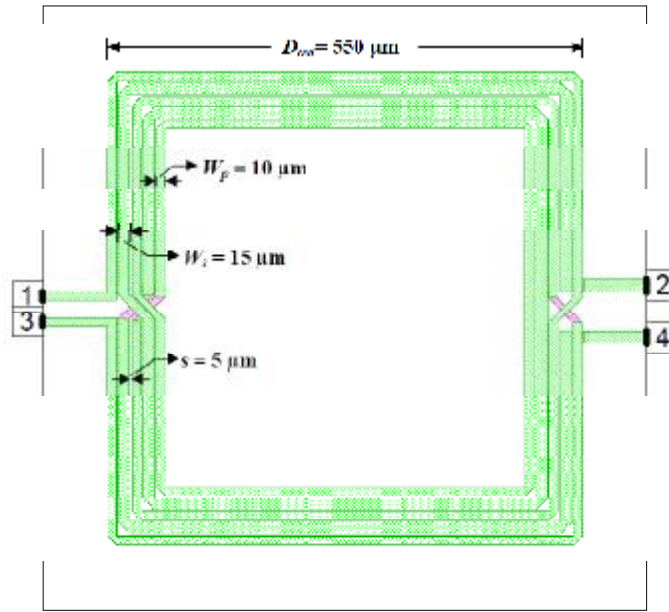


(b)

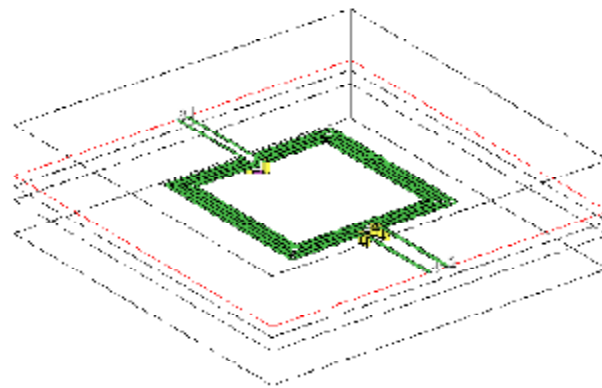
Figure (5): EMSight setup for on-chip (1:1) balun transformer, (a) Top view, and (b) Orthogonal view.

To reduce the size of the on-chip balun transformer (area-efficient), the primary and secondary coils of this transformer are turned into two windings instead of one winding.

In addition, to minimize the losses (heat) that is generated due to the orthogonal edge at each corner of the primary and secondary traces of the transformer; the orthogonal edge is converted to lapped edge. Figure 6 shows the on-chip balun transformer design after improvement.



(a)



(b)

Figure (6): EMSight setup for on-chip (1:1) improvement balun transformer (a) Top view, and (b) Orthogonal view.

SIMULATION RESULTS

The proposed power amplifier is designed and simulated using microwave office 2009(version 9.00) [15], with all the devices optimized to achieve the required Bluetooth performance. Figure (7) shows the simulated output power,

power gain, and power-added-efficiency versus input power at a frequency of 2.4 GHz. The PA provides 21.57 dBm of output power with a maximum gain of 16.57 dB and a PAE of 65.59% for an input power of 5 dBm as shown in Figure (7)

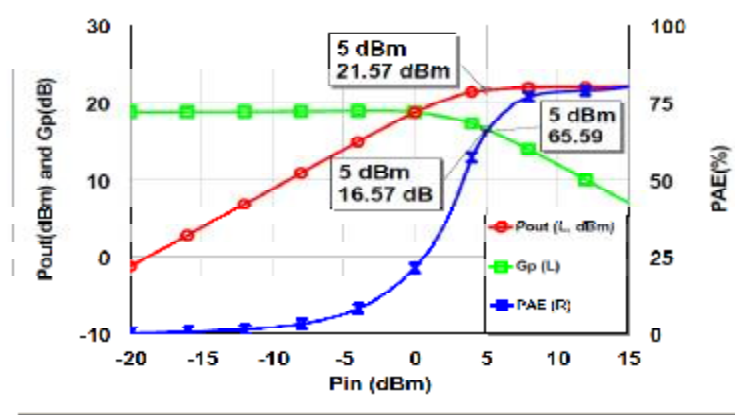


Figure (7): Output power (P_{out}), power gain (G_p), and power-added-efficiency (PAE) versus input power (P_{in}) at a frequency of 2.4 GHz for the proposed PA.

The simulated performance of the PA as a function of frequency for an input power of 5 dBm is presented in Figure (8). As shown from this figure, the gain of the prototype PA remains almost flat over the class-1 Bluetooth band, which is from 2.4 GHz to 2.48 GHz. The minimum PAE is 65.59% while the output power is above 21.39 dBm for the entire class-1 Bluetooth band, thereby, fulfilling the 20-dBm output power requirement.

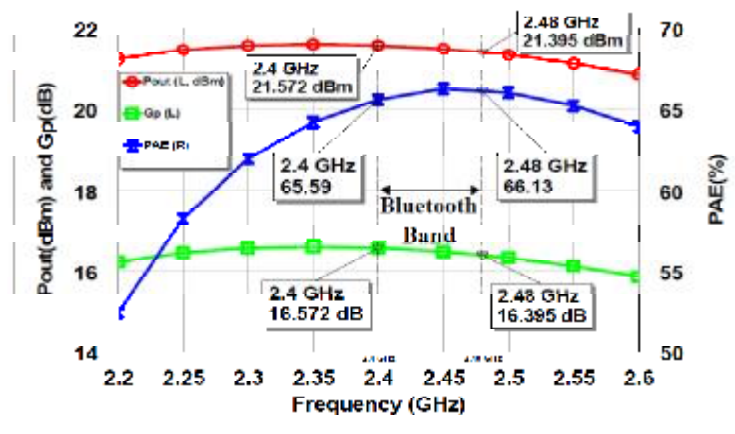


Figure (8): Output power (P_{out}), power gain (G_p), and power-added-efficiency (PAE) versus frequency for P_{in} of 5 dBm, for the proposed PA.

In order to estimate the linearity of the proposed PA, the compression characteristics are plotted in Figure (9). As shown from this figure, the power amplifier reaches its output 1dB compression at 20.78 dBm, with an input power level of 2.9 dBm. The BSIM3v3.3 model [16] for MOSFET transistor is used in the power amplifier simulation.

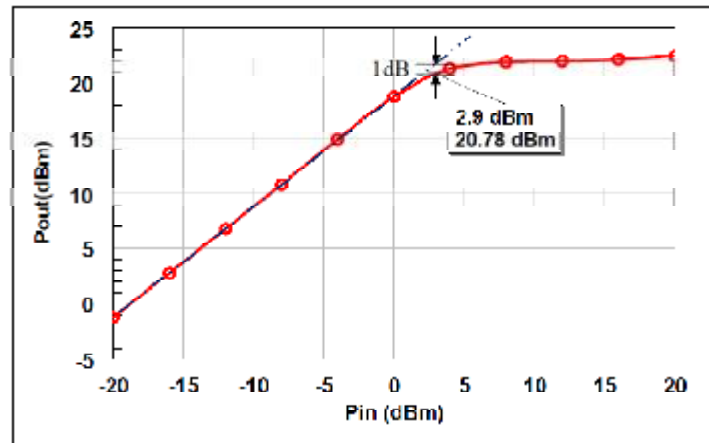


Figure (9): Compression characteristic (1-dB compression point) at a frequency of 2.4 GHz.

Finally, to verify the feasibility of the segmentation idea in the balun transformer performance improvement, a square transformer with segmentations is simulated using EMSight simulator. EMSight simulator is an electro-magnetic solver provided with Microwave Office (MWO) 2009 RF/Microwave software tools. The geometrical parameters for balun transformer and the simulation results are summarized, previously, AS in Table (3).

Table (4) shows the geometrical parameters and the simulation results for the improvement balun transformer. A comparison between the results in Table (3) and Table (4) show that the values of L_p , L_s , Q_p , Q_s , k , and IL_{min} are remained approximately the same, with reduction in the area required for implementing the transformer.

Table (4): Geometrical parameters and simulation results for on-chip improvement balun transformer.

Geometrical parameters		Simulation results	
$D_{out}(\mu\text{m})$	550	$L_p(\text{nH})$	2.8
$W_p(\mu\text{m})$	10	$L_s(\text{nH})$	3.31
N_{seg}	3	Q_p	11.7
$W_s(\mu\text{m})$	15	Q_s	12
N_{seg}	2	k	0.68
$s(\mu\text{m})$	5	$IL_{min}(\text{dB})$	1.22

CONCLUSIONS:

The design and simulation of a power amplifier for class-1 Bluetooth system in 0.13 μm CMOS technology is presented. By using differential topology with two ideal transformers, P_{o1dB} of 20.78 dBm can be achieved at 2.9 dBm input power. The proposed power amplifier can deliver 21.57 dBm output power to a 50 Ω load at 2.4 GHz with 65.59 % power-added-efficiency (PAE) and 16.57 dB from 1V

supply. The designed on-chip balun transformer used in this work plays two roles: First, it is used to transform the 50 Ω load. Second, it converts a differential signal into single-ended signal so that it can be connected to the antenna directly, and it converts a single-ended signal to differential signal in the input side.

The characteristics of the PA, accompanied by those of the other Bluetooth PAs, are summarized in Table 5. As a comparison with other listed CMOS PAs for Bluetooth applications, this amplifier has the highest power-added-efficiency, lowest supply voltage, good output power, medial linearity, and no external components are required.

Finally, all the results are obtained from the simulation, and there is the need for fabricating this proposed design to verify the results, practically, presented in this work.

Table (5): Comparison with other Bluetooth PAs.

Reference	Year	CMOS technology	P_{out} (dBm)	Gp (dB)	PAE (%)	V_{DD} (V)	Class	External component
[15]	2010	0.18μm	19.2	15	27.8	3.3	E	Yes
[07]	2010	0.18μm	21.09	16.09	57	1.8	E	Yes
[03]	2011	0.18μm	25.1	20.1	54.2	1.8	E	No
[16]	2013	0.13 μm	22	-	38	2.5	E	No
This work*	2013	0.13 μm	21.57	16.57	65.59	1.0	E	No

*Simulation

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